LOW POWER DUAL-PORTS IN ADVANCED HANDSET APPLICATIONS

APPLICATION NOTE AN-410

Background

As the demand for high-end wireless handsets continues to rise, the ability for OEMs and ODMs to quickly and cost effectively develop new, increasingly advanced models becomes more and more important. Also, it is equally important that these new models take advantage of the performance supported by emerging wireless data standards so that the value of the "killer apps" they bring to the market is fully realized. This application note discusses one solution that addresses these issues and the value that the IDT70P248 Low Power Dual-Port brings to these types of products.

Dual-Processor Architecture

The high-end, multimedia functions included in today's wireless handsets bring with them more robust processing requirements. As a result, many of the features demanded by consumers out-pace the processing horsepower provided by available baseband processors, including those with integrated ARM cores. In cases such as this, an additional applications processor is required to help off-load some of the processing associated with multimedia applications and the use of a full operating system and application suite.

In addition to the higher level of processing it provides, there are two other benefits of adopting the dual-processor approach shown in Figure 1. First, it is a highly modular architecture that allows a single design to be used as the basis for numerous models supporting various peripheral, performance and wireless standard requirements. For example, a fixed applications block, with its supporting peripheral components, can be used in conjunction with a variety of different baseband processors, giving OEMs the ability to quickly target multiple geographies using only a limited amount of design resources. Second, this approach relies primarily of off-the-shelf components, which eliminate the need for long and costly ASIC/FPGA development cycles.

Inter-processor Communication

Once a dual-processor architecture has been adopted, a means of inter-processor communication must be established so that data can be transferred back and forth from the air I/F and baseband processor to the applications processor. While a number of methods can be employed to facilitate this communication, the IDT70P248 is the only off-the-shelf solution that provides both the bandwidth necessary to support data rates greater than 1Mbps (see Table 1) and the aggressive power and packaging targets demanded by these kinds of applications (see Table 2). Moreover, the Interrupt functionality provided by the IDT70P248 can be used to aid in software flow control and as a polling mechanism to prevent both ports from being simultaneously accessed, keeping the average power consumed to minimum.

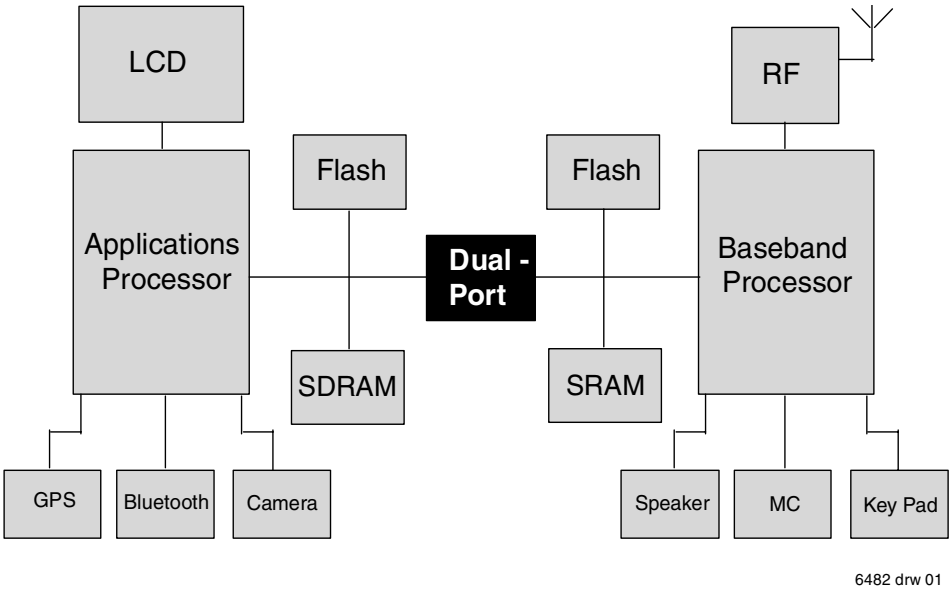

Figure 1. High-end Wireless Handset

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Low Power Operation

The IDT70P248 has been optimized to consume very little power both when operational and when in standby mode (see Table 3). By supporting ultra-low operating and standby currents and a 1.8V core voltage, the IDT70P248 extends both the talk time and the standby time of the handset by limiting the power drawn from the battery under all conditions.

Advanced Functionality

In addition to providing high-performance, low-power communication between the two processors, the IDT70P248 also features two specialty functions designed specifically for the wireless handset market. The Input Read Register and Output Drive Register allow both of the processors to monitor and/or drive a number of external binary input devices without sacrificing any additional pins. This increases the overall flexibility of the solution by allowing the limited number of controls pins on the two processors to be used for other purposes.

		UART	USB1.1	Dual-Port
GPRS	171.2 kbps			
cdma2000 1x	307 kbps			
EDGE	384 kbps			
cdma2000 3x	2 Mbps			
W-CDMA	2 Mbps			
cdma2000 1xEV-DO	2.4 Mbps			
cdma2000 1xEV-DV	4.8 Mbps			
WCDMA (HSPDA)	8-10 Mbps			
802.11b	11 Mbps			

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Table 1. Inter-processor Communication Bandwidth

Symbol	Description	IDT70V24VL	IDT70T24L	IDT70P248	USB 2.0 Host/Controller	USB1.1 Host/Controller
V_{DD}	Supply Voltage	3.0	2.5	1.8V	3.3V	3.3V
I_{DD}	Operating Current	75mA	50mA	15mA	345mA	50mA
I_{SB3}	Standby Current	42uA	25uA	2uA	10.4mA	500uA
P	Operating Power	225mW	125mW	27mW	1.14W	165mW
p	Standby Power	126uW	63uW	4uW	34mW	1.6uW
	Package Size	64mm^2	64mm^2	36mm^2	64mm^2	100mm^2

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Table 2. Package Size and Power Consumption Comparison

Symbol	Parameter	Typ.	Max.	Unit
I_{DD}	Dynamic Operating Current (Both Ports Active - CMOS Level Inputs)	15	25	mA
I_{SB3}	Standby Current (Both Ports - CMOS Level Inputs)	2	8	uA

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Table 3. IDT70P248 Operating and Standby Current Levels

Input Read Register

The Input Read Register (IRR) of the IDT70P248 captures the status of two external binary input devices connected to the Input Read pins (e.g. DIP switches). This allows either processor to monitor the status of two external devices using only those pins already used to I/F with the IDT70P248. When access to the IRR is enabled, the contents of the IRR are read from the IDT70P248 as a standard memory access to address x0000 from either port and the data is output via the standard I/Os. The IRR supports inputs up to 3.5V ($V_{IL} \leq 0.4V$, $V_{IH} \geq 1.4V$).

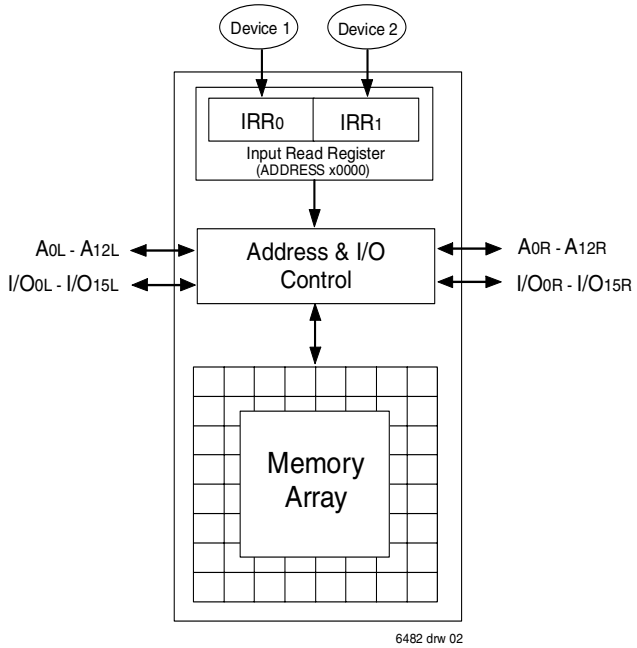

Figure 2. IDT70P248 Input Read Register

Output Drive Register

The Output Drive Register (ODR) of the IDT70P248 determines the state of up to five external binary-state devices by providing a path to V_{SS} for the external circuit. This gives either processor the ability to control up to five external devices (e.g. LEDs) without sacrificing any additional control signals. The five external devices supported by the ODR can operate at different voltages ($1.5V \leq V_{SUPPLY} \leq 3.5V$), but the combined current of the devices must not exceed 40mA (8mA I_{MAX} for each external device). When the access to the ODR is enabled, the status of the ODR bits is set using standard write accesses to the IDT70P248 from either port to address x0001 with a "1" corresponding to "on" and a "0" corresponding to "off". The status of the ODR bits can also be read (without changing the status of the bits) via a standard read to address x0001.

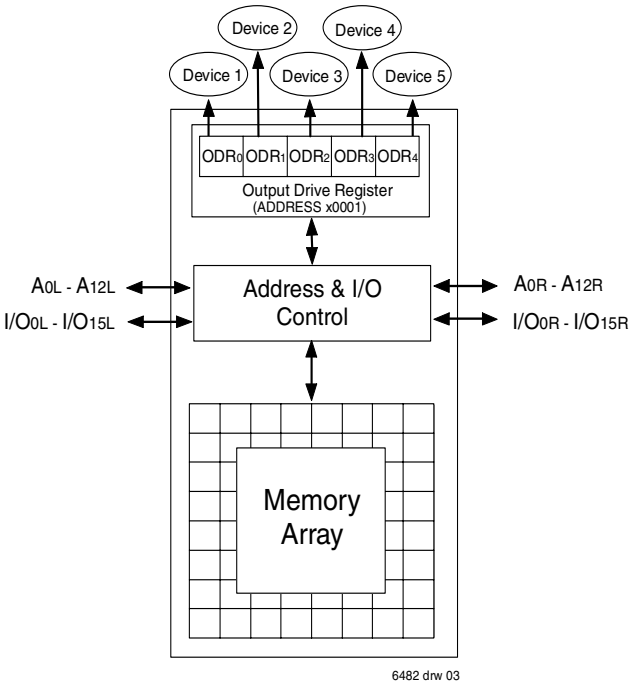

Figure 3. IDT70P248 Output Drive Register

Summary

As shown here, the dual-processor architecture provides OEMs and ODMs with a powerful, flexible, and cost effective approach to high-end handset designs. Using the IDT70P248 as the communication link between the application and baseband processors further optimizes the performance and power consumption of these designs. By taking advantage of this highly specialized device from IDT, the industry's leading supplier of multi-ports, wireless handset manufacturers can shorten their design cycles while still presenting their customers with a wide array of high performance products.

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