Introduction

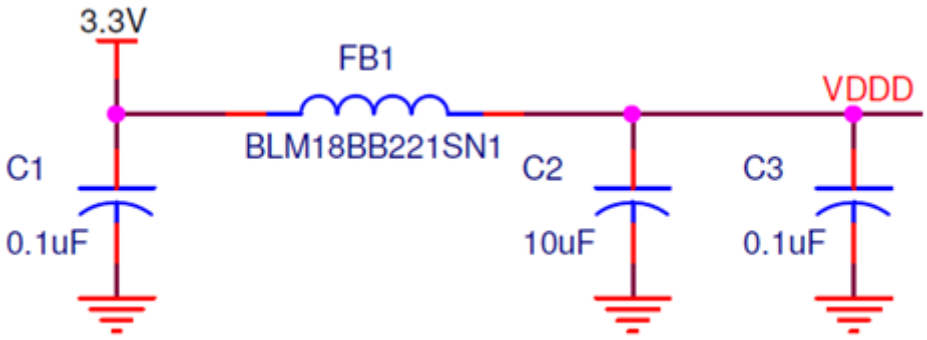
This application note describes the procedure used within the Timing and Synchronization (TSD) division of IDT to analyze the PSNR for its devices. Power supply noise rejection (PSNR) is a measurement of how well a circuit rejects noise from various frequencies which are coupled into the power supply. In actual high speed analog and digital circuitry, the power supply pins are vulnerable to random noise Most customer designs use linear voltage regulators or switching voltage regulators as the power supply for ICs. Linear regulators will almost always get input voltage from a switching DC/DC converter. Therefore, power supply noises in a customer board typically come from the switching noise of the power supply and coupling from other high-frequency sections of the circuit board.

Many of the problems facing PCB designers today are related to power supply noise. There are guidelines that can be used to solve simple issue. For more complex issues, a better understanding and consideration of all the parameters will be required to provide a clean solution. For this reason, it is essential to understand the PSNR of the clock devices. This can assist in designing the correct bypassing and decoupling for the system.

Power Supply Filtering Topology

Figure 1 is a simplified 3-component power supply filtering circuit that is recommended for a power rail. It consists of a 0.1µF capacitor (C1) a ferrite bead (FB1) and a 10µF capacitor (C2). While C1, FB1 and C2 are for the power rail, C3 is used for each power pin supplied by this rail. If a power rail supplies multiple power pins, each power pin will have a 0.1µF capacitor for decoupling.

Figure 1. Power Supply Filtering Circuit Topology



The ferrite bead above is any surface-mount bead with sufficient current rating for the circuits supplied. Please refer to AN-805 for ferrite bead recommendations.

Effectiveness Study of the Noise Rejection Circuits

The frequency response is used to study the attenuation capability the above circuit demonstrates on different frequency elements of a signal (noise). In the following sections of this application note, frequency response of the circuit is plotted by sweeping C1, C2 and C3, respectively:

Figure 2: Sweeping C1 while keeping C2 = 10µF, C3 = 0.1µF – Optimal value for C1 is 0.1µF

Figure 3: Sweeping C2 while keeping C1 = 0.1µF, C3 = 0.1µF – Optimal value for C2 is 10µF

Figure 4: Sweeping C3 while keeping C1 = 0.1µF, C2 = 10µF – Optimal value for C3 is 0.1µF

Figure 2. Sweeping C1 while keeping C2 = 10µF, C3 = 0.1µF

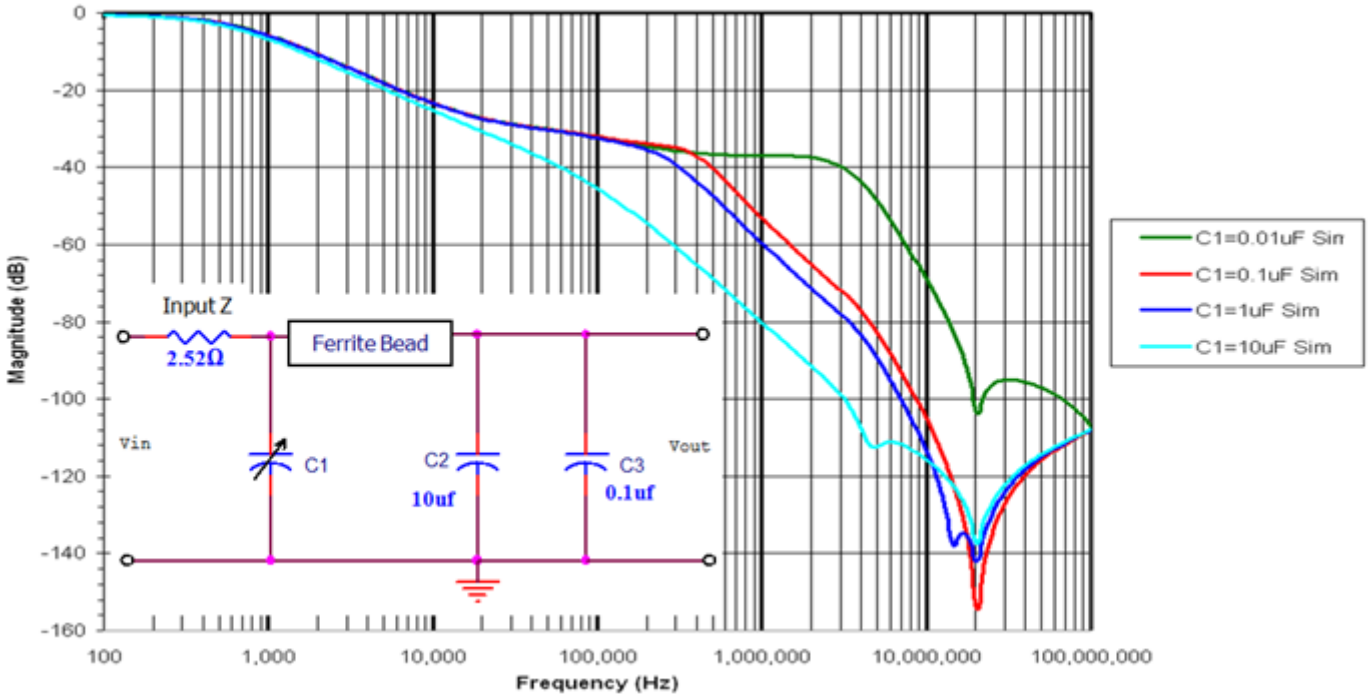


Figure 3. Sweeping C2 while keeping C1 = 0.1µF, C3 = 0.1µF

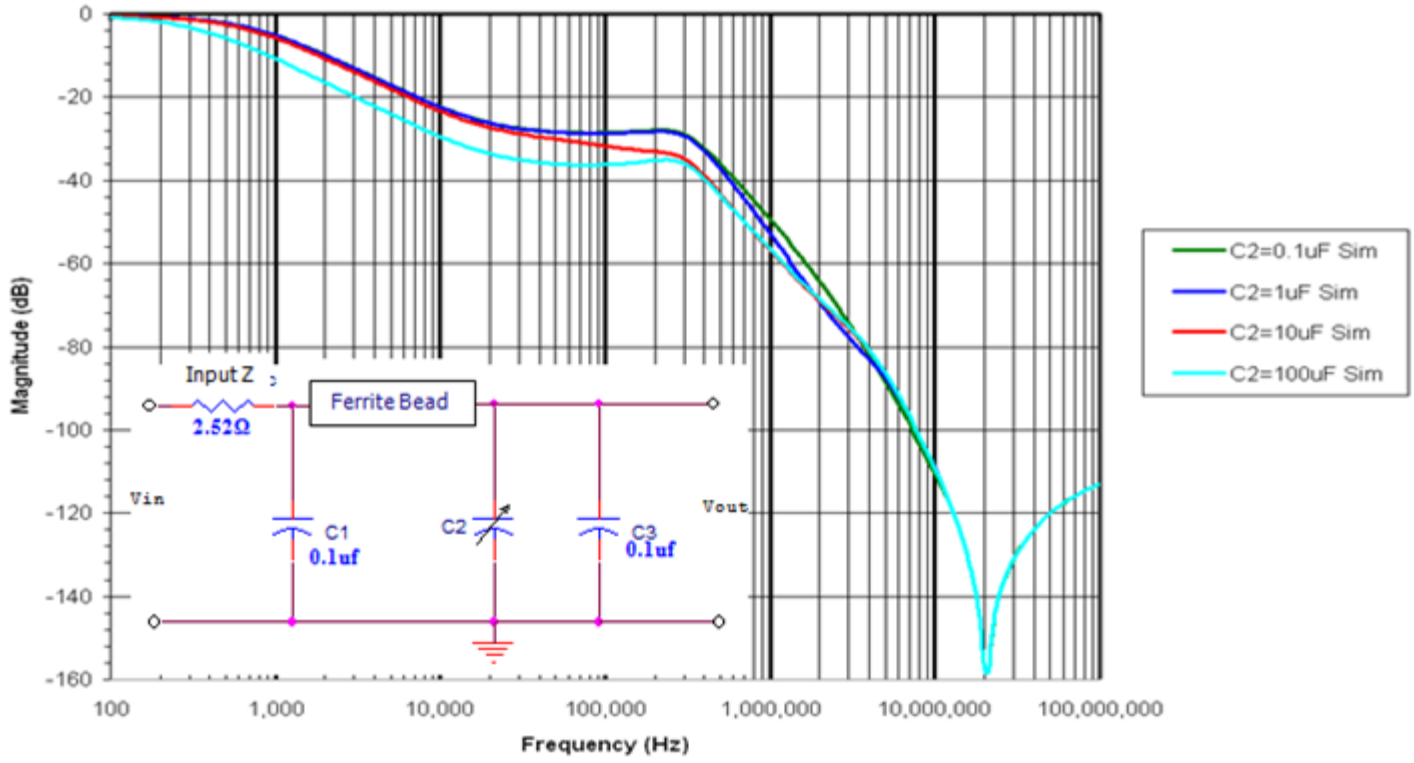
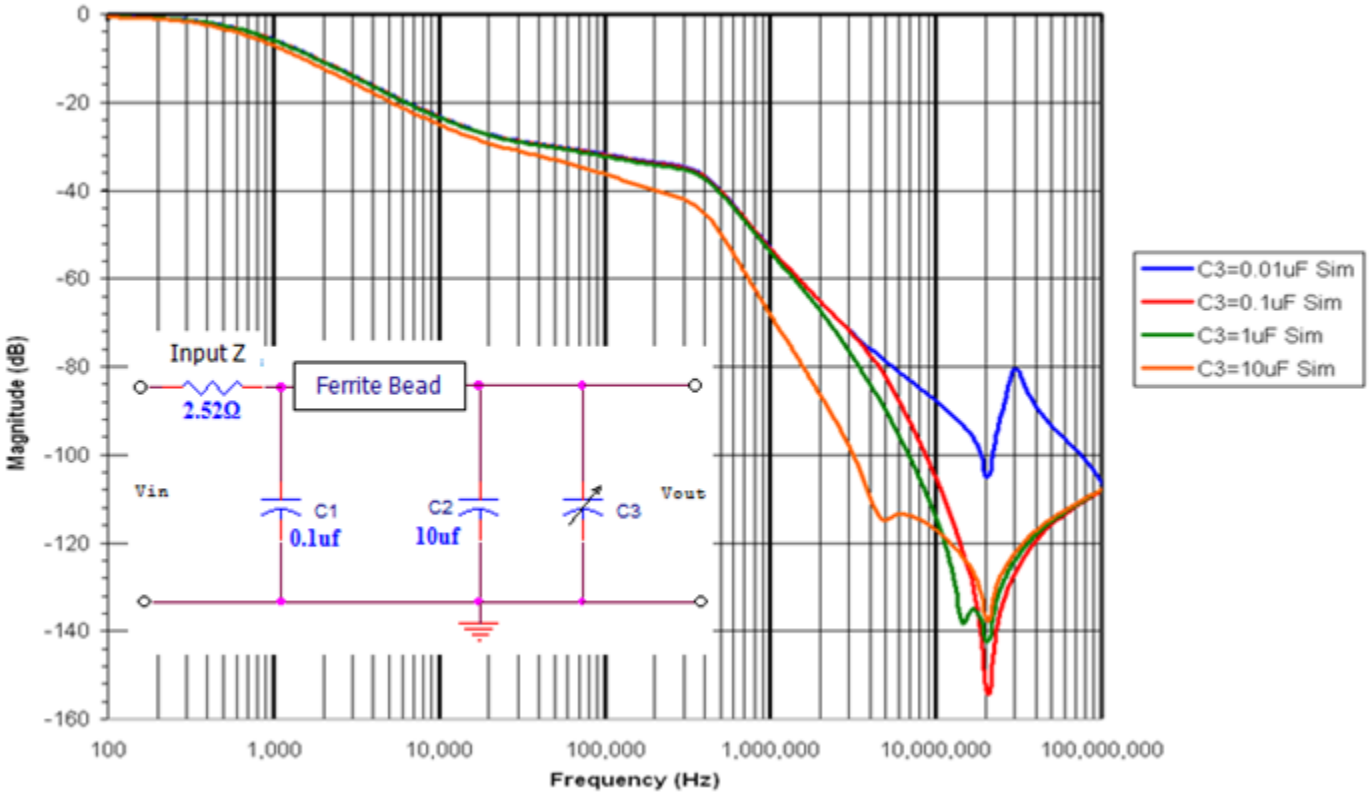


Figure 4. Sweeping C3 while keeping C1 = 0.1µF, C2 = 10µF

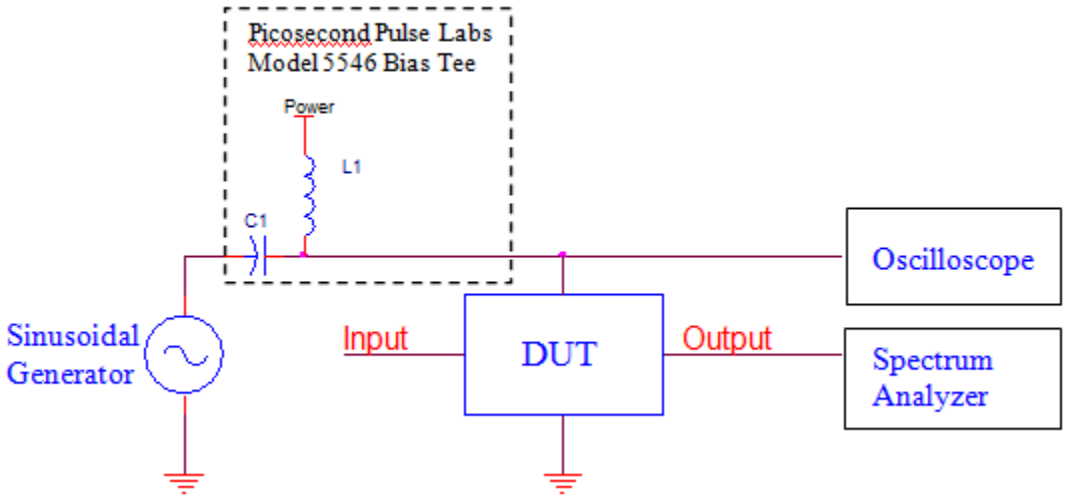


Power Supply Noise Rejection Measurements

PSNR is measured by injecting a sinusoidal signal of a known amplitude and frequency onto the various power supply pins of the devices. Many of the devices in the TSD portfolio contain multiple power supply pins. The two of interest are the core power pin and the analog power pin. The core power pin primarily supplies voltage to all PLL peripherals while the analog power pin supplies the voltage to the PLL. Each power pin should be analyzed independently, and noise should be applied to one power pin at a time.

The technique used for applying the injected frequency into the device supply uses an inductor which presents a high AC impedance back to the supply. Then a signal from a generator is injected through a capacitor after the inductor at the pin of the DUT. Refer to Figure 1. Both the input and output should be monitored with an oscilloscope and Spectrum analyzer. The oscilloscope is used to ensure the signal amplitude while the spectrum analyzer is used to measure the deterministic jitter.

Figure 5. PSNR Schematic



In order to analyze the performance of the device, initially all external bypass and decoupling capacitors should be removed. A 50mV signal is swept from a start to a stop frequency. The 1kHz to 50MHz sweep range covers most of standard frequencies which occur in typical applications.

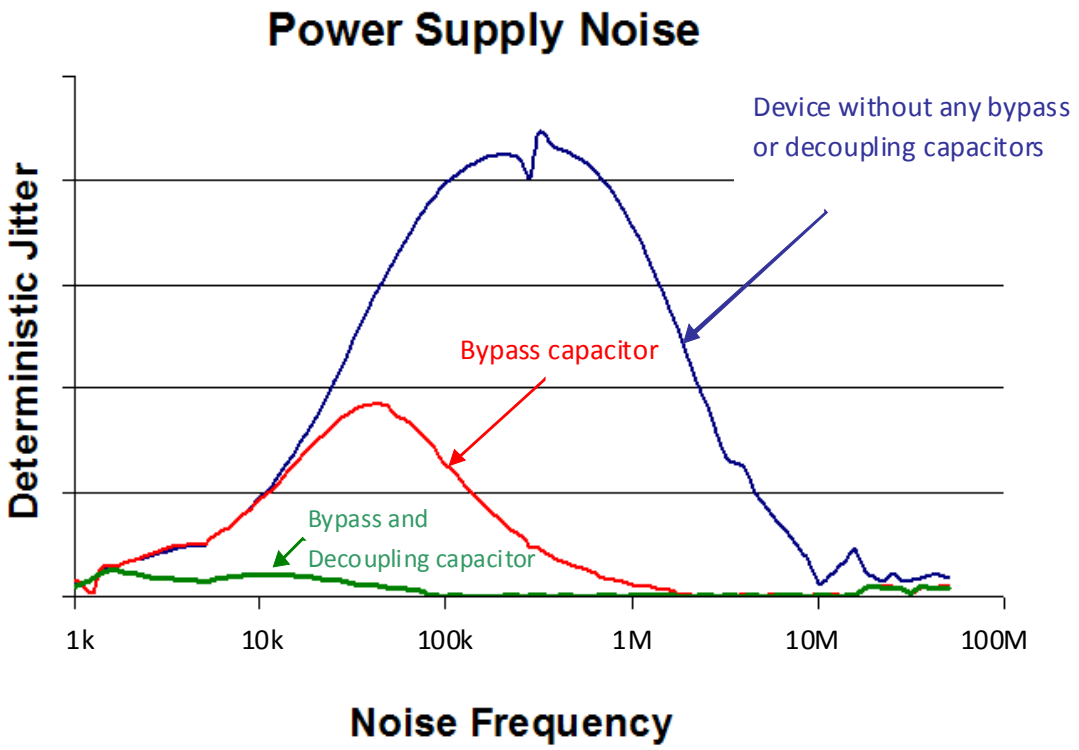
Table 1. PSNR Configuration

Power Pin	Temperature (°C)	Signal Amplitude (mV)	Start Frequency (kHz)	Stop Frequency (MHz)
Core Voltage	25	50	1	50
Analog Voltage	25	50	1	50

The following graph represents three tests of PSNR data. First, the device was swept without any decoupling or bypass capacitors. Notice, the deterministic jitter peaked at approximately 400kHz. Next, a 0.1µf bypass capacitor was added and the noise decreased significantly. Lastly, in addition to the 0.1µf, a 10µf capacitor was added and majority of the noise is filtered. Refer to Figure 2.

In conclusion, the combination of a 0.1µf and 10µf capacitor will attenuate some of the noise generated by a switching power supplies. For many of the TSD devices, a power supply filter with a ferrite bead is recommended. This will attenuate noise between 100kHz and 600kHz.

Figure 6. Deterministic Jitter versus Noise Frequency

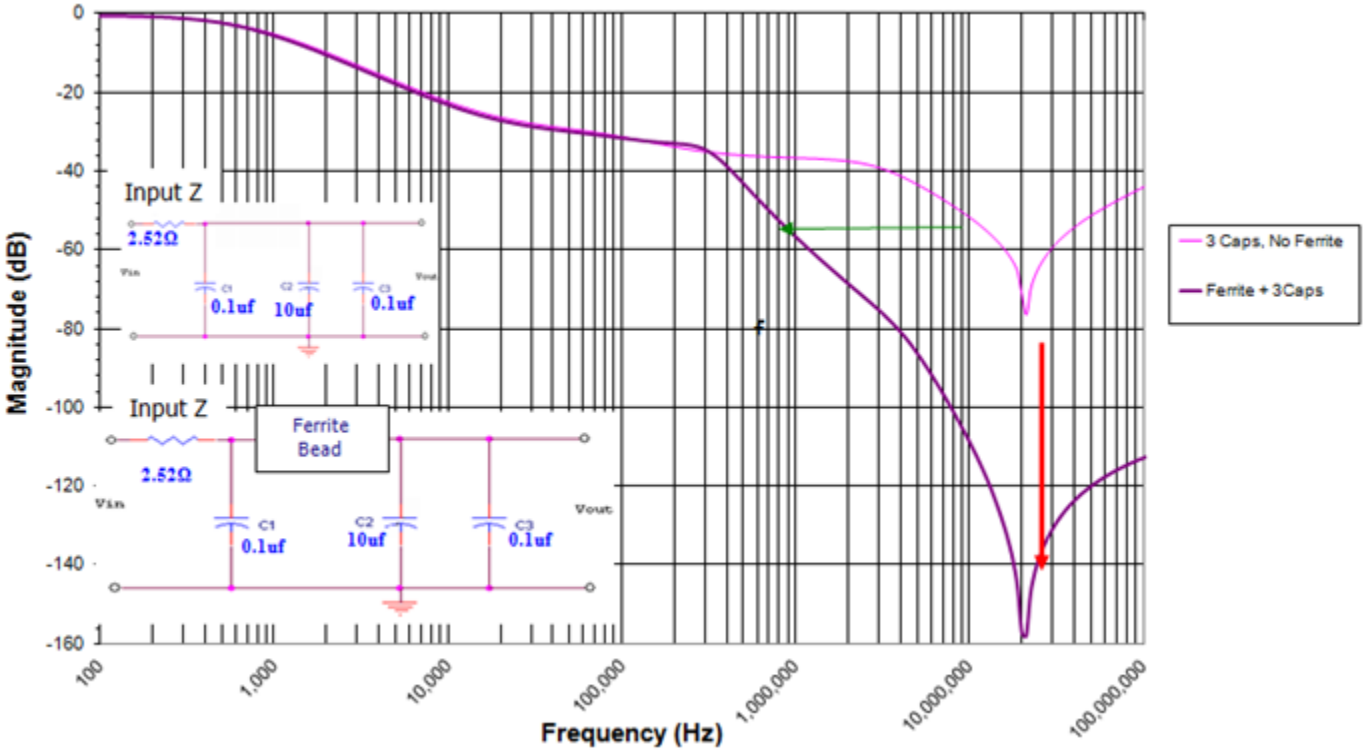


Summary

This application note proposes a simple power supply noise rejection topology consisting of two capacitors and a ferrite bead. By sweeping the values of the capacitors, a noise-filtering circuit with recommended component values is provided in Figure 1. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

Overall, this filtering circuit provides significant noise attenuation in frequency range of 10KHz to 100MHz compared with a 0.1µF-only filtering. Figure7 shows the comparison between a 0.1µF-only filter and Figure 1 filtering circuit.

Figure 7. Noise Rejection Comparison: 0.1µF Capacitor Only vs Filtering Circuit by Figure 1



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