

### Introduction

High Speed Current Steering Logic (HCSL) is the de facto output types for PCI Express applications and Intel chipsets. It is an open emitter output with a 15mA current source and requiring 50Ω external resistor to ground for the output to be switching. In PCI Express 1.1, HCSL is specified to have 50Ω impedance single-ended or 100Ω differential. From PCI Express 2.0, 85Ω differential impedance is added into PCI Express specifications.

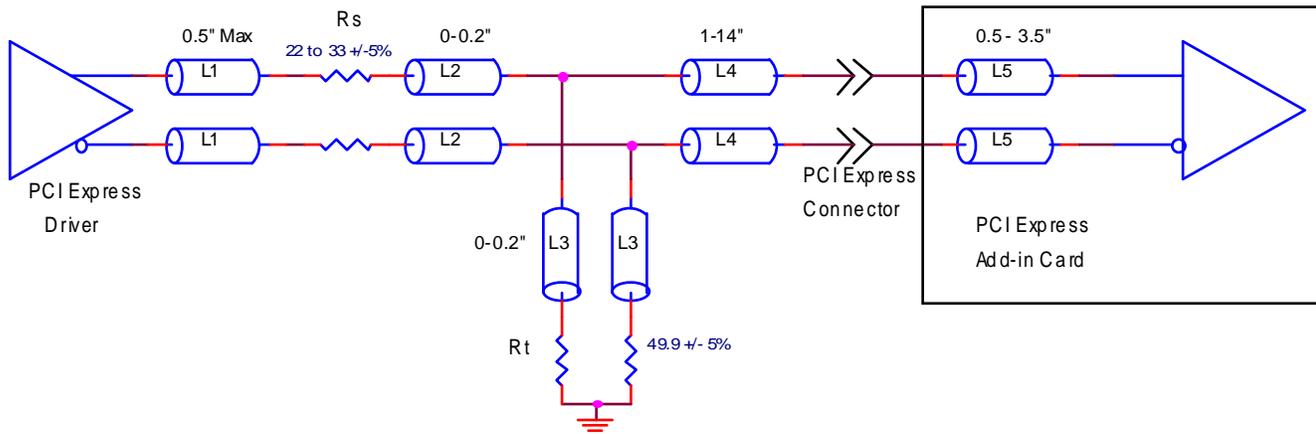
### Standard HCSL Terminations

A standard HCSL termination calls for a 50Ω resistor from each lead to ground. A series resistor is also added to help reduce overshoot and signal ringing. The following two examples show HCSL termination topology.

### HCSL Terminations for Applications Where Driver and Receiver are on Separate PCBs

The figure below represents the recommended source termination for applications where the driver and receiver will be on separate PCBs. It also shows the standard for PCI Express and HCSL output types. All traces should be 50Ω impedance single ended or 100Ω differential.

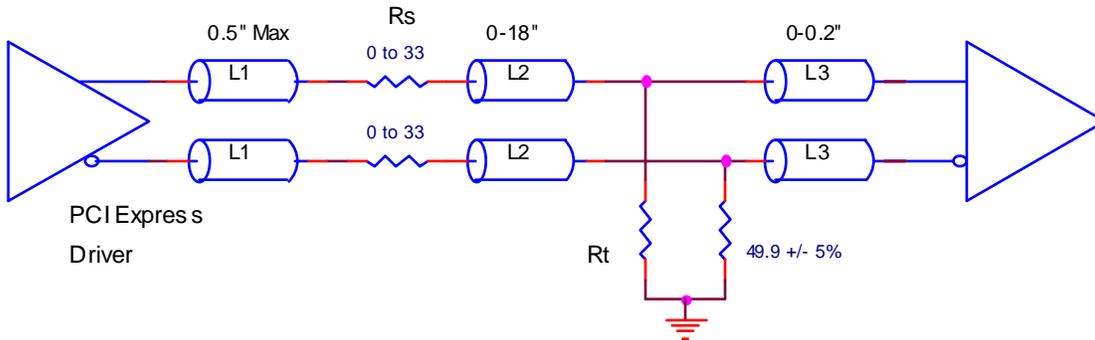
**Figure 1. Termination for Applications Where Driver and Receiver will be on Separate PCBs**



### HCSL Terminations for Applications Where Driver and Receiver are on the Same PCB

The figure below represents is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor ( $R_s$ ) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from  $0\Omega$  to  $33\Omega$ . All traces should be  $50\Omega$  impedance single ended or  $100\Omega$  differential.

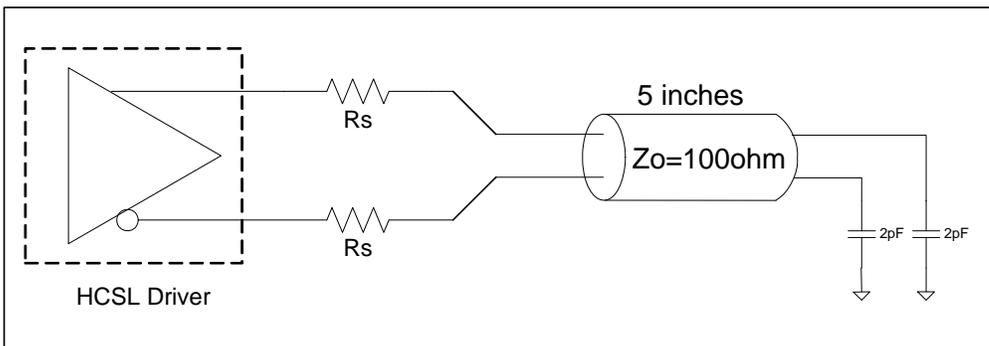
**Figure 2. Termination for Applications Where a Point-to-Point Connection can be Used**



### HCSL Terminations for IDT Low-Power PCI Express Clock Generators and Buffers

IDT provides a wide selection of PCI Express clock solutions. The new Low Power (LP-HCSL) and Ultra Low Power (ULP-HCSL) series of IDT PCI Express clock generators, buffers and multiplexers use a current source in the driver, instead of a voltage source in some old devices. Thus they require only series resistors to achieve  $85\Omega$  or  $100\Omega$  differential impedance terminations, as shown in Figure 3 below, in which  $50\Omega$  resistor to the ground is no longer needed. This will save power consumption of the device significantly. In addition, termination is simplified. LP-HCSL devices include 9FGL0x31/0x41 and 9DBL0x31/0x41, where  $x = 2, 4, 6, 8$ . ULP-HCSL devices include 9FGV0x31/0x41 and 9DBV0x31/0x41, where  $x = 2, 4, 6, 8$ . Refer to each device datasheet for technical details. The figure below represents the recommended source termination for applications using IDT low-power (9FGLxxx/9DBLxxx) or ultra low-power (9FGVxxx/9DBVxxx) series PCI Express Clock generators and buffers.

**Figure 3. Termination for Applications using LP-HCSL or ULP-HCSL PCIe Clock Generators and Buffers**



#### Alternate Differential Output Terminations

$R_s$	$Z_o$	Units
33	100	$\Omega$
27	85	



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