

### General Description

The 840NT4-01 is clock generator designed to provide ethernet and USB clocks for Freescale B4/ T4-based systems. The 840NT4-01 utilizes IDT's FemtoClock NG<sup>®</sup> PLL technology to synthesize eight low phase-jitter Ethernet reference clocks. The clock generator also provides a 24MHz USB reference clock and a 25MHz reference output.

### Recommended Application:

- Freescale B4/ T4 Ethernet /USB clock generator

### Output Features:

- Five LVCMOS 125MHz Ethernet outputs
- Three LVCMOS 25MHz/ 125MHz Ethernet outputs
- One LVCMOS 24MHz USB output
- One LVCMOS 25MHz REF output

### Features

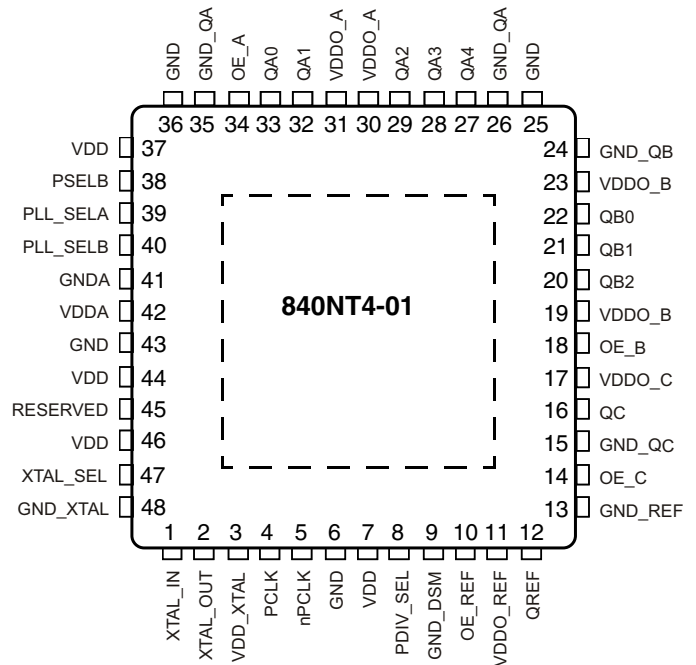
- Ten LVCMOS clock outputs:
  - Five LVCMOS 125MHz Ethernet outputs
  - Three LVCMOS 25MHz /125MHz Ethernet outputs
  - One LVCMOS 24MHz USB output
  - One LVCMOS 25MHz REF output
- QREF output can be used to drive other clock drivers, saving a crystal
- Selectable crystal or differential LVPECL input
- RMS Phase Jitter, 125MHz, integration range 12kHz - 20MHz: 0.60ps (typical)
- Cycle-to-Cycle jitter: 20ps (typical)
- Flexible voltage supply modes; supports legacy and future system requirements, minimizes power consumption
  - Core voltage:  $V_{DD}$ ,  $V_{DD\_XTAL}$ ,  $V_{DDA}$
  - Output voltage:  $V_{DDO\_A}$ ,  $V_{DDO\_B}$ ,  $V_{DDO\_C}$ ,  $V_{DDO\_REF}$
  - Core / Output
    - 3.3V / 3.3V
    - 3.3V / 2.5V
    - 3.3V / 1.8V
    - 2.5V / 2.5V
    - 2.5V / 1.8V
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

**Table 1. Output Frequency Table**

| PD* (MHz) | PSELB | PLL_SELA | PLL_SELB | F <sub>OUT</sub> (MHz) |         |    |      |
|-----------|-------|----------|----------|------------------------|---------|----|------|
|           |       |          |          | QA[4:0]                | QB[2:0] | QC | QREF |
| 25        | 0     | 0        | 0        | 125                    | 125     | 24 | 25   |
| 25        | 1     | 0        | 0        | 125                    | 125     | 24 | 25   |
| 25        | 0     | 0        | 1        | 125                    | 25      | 24 | 25   |
| 25        | 1     | 0        | 1        | 125                    | 25      | 24 | 25   |

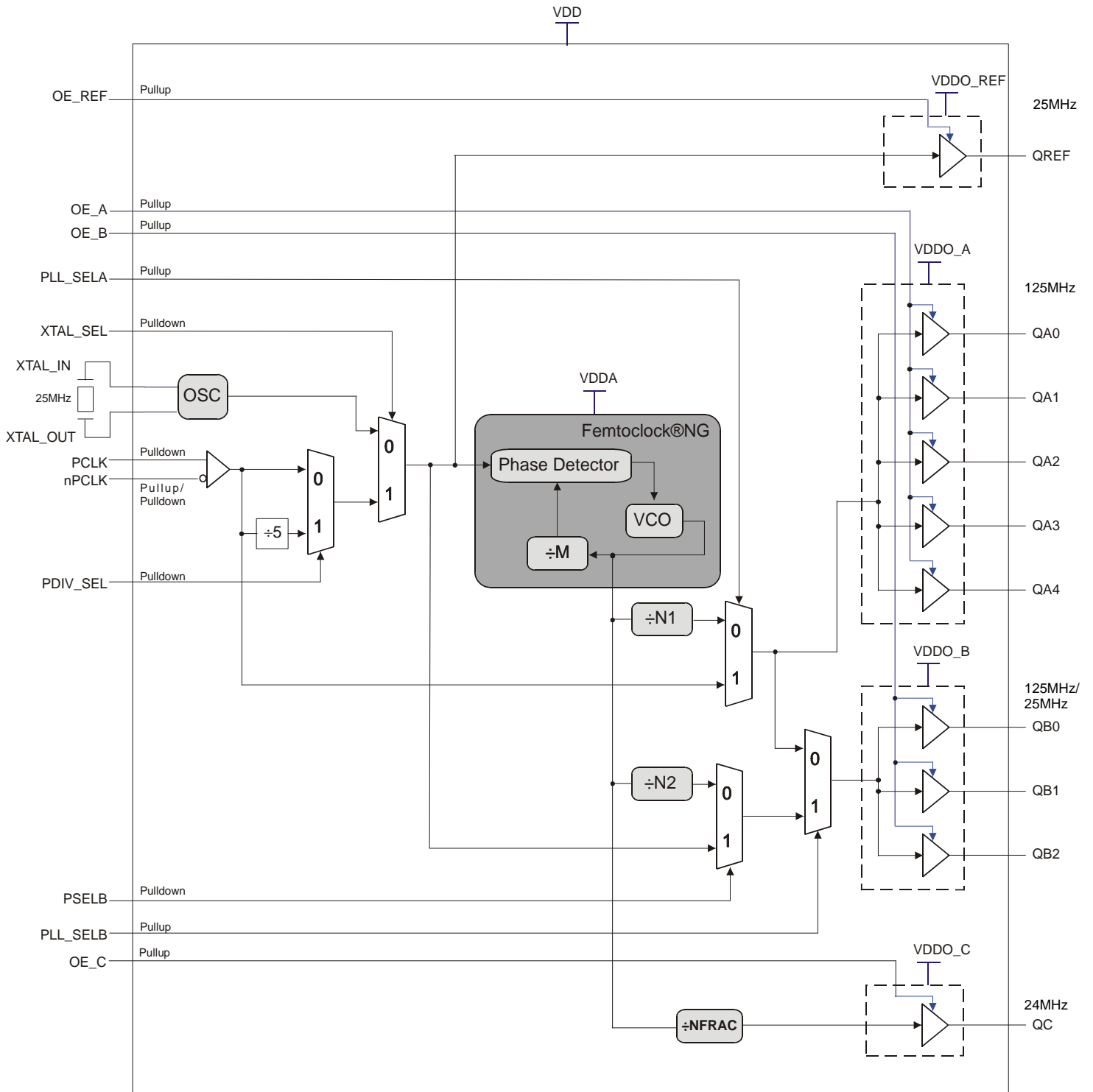
\*PD = Phase Detector input frequency.

### Pin Assignment



**48-lead, 7.0mm x 7.0mm VFQFN**

# Block Diagram



## Pin Description and Pin Characteristic Tables

**Table 2. Pin Descriptions<sup>1</sup>**

| Number | Name                 | Type   |                     | Description   |
|--------|----------------------|--------|---------------------|---|
| 1      | XTAL_IN              | Input  |                     | Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.   |
| 2      | XTAL_OUT             | Input  |                     |   |
| 3      | V <sub>DD_XTAL</sub> | Power  |                     | Power supply pin for XTAL.  |
| 4      | PCLK                 | Input  | Pulldown            | Non-inverting external 25MHz differential LVPECL reference input. LVPECL input levels.  |
| 5      | nPCLK                | Input  | Pullup/<br>Pulldown | Inverting external 25MHz differential LVPECL reference input. LVPECL input levels.  |
| 6      | GND                  | Power  |                     | Power supply ground.  |
| 7      | V <sub>DD</sub>      | Power  |                     | Core supply pins.   |
| 8      | PDIV_SEL             | Input  | Pulldown            | Selects input for PCLK (LOW) or ÷5 pre-divider (HIGH). LVCMOS/LVTTL interface levels.   |
| 9      | GND_DSM              | Power  |                     | Ground pin for Delta Sigma Modulator.   |
| 10     | OE_REF               | Input  | Pullup              | Output enable for QREF output. The output is placed in a high-impedance mode on disable. LVCMOS/LVTTL interface levels.           |
| 11     | V <sub>DDO_REF</sub> | Power  |                     | Output power supply for QREF output.  |
| 12     | QREF                 | Output |                     | Single-ended 25MHz, reference clock output. LVCMOS/LVTTL interface levels.  |
| 13     | GND_REF              | Power  |                     | Ground pin for QREF clock output.   |
| 14     | OE_C                 | Input  | Pullup              | Output enable for QC output. The QC output is placed in a high-impedance mode on disable. LVCMOS/LVTTL interface levels.          |
| 15     | GND_QC               | Power  |                     | Ground pin for QC clock output.   |
| 16     | QC                   | Output |                     | Single-ended 24MHz, USB clock output. LVCMOS/LVTTL interface levels.  |
| 17     | V <sub>DDO_C</sub>   | Power  |                     | Output power supply for QC output.  |
| 18     | OE_B                 | Input  | Pullup              | Output enable for Bank QBx outputs. The output bank is placed in a high-impedance mode on disable. LVCMOS/LVTTL interface levels. |
| 19     | V <sub>DDO_B</sub>   | Power  |                     | Output power supply for Bank QBx clock outputs.   |
| 20     | QB2                  | Output |                     | Single-ended 125MHz or 25MHz clock outputs. LVCMOS/LVTTL interface levels.  |
| 21     | QB1                  | Output |                     |   |
| 22     | QB0                  | Output |                     |   |
| 23     | V <sub>DDO_B</sub>   | Power  |                     | Output power supply for Bank QBx clock outputs.   |
| 24     | GND_QB               | Power  |                     | Ground pin for Bank QBx clock outputs.  |
| 25     | GND                  | Power  |                     | Power supply ground.  |
| 26     | GND_QA               | Power  |                     | Ground pin for Bank QAx clock outputs.  |
| 27     | QA4                  | Output |                     | Single-ended output clocks, optimized at 125MHz. LVCMOS/LVTTL interface levels.   |
| 28     | QA3                  | Output |                     |   |
| 29     | QA2                  | Output |                     |   |
| 30     | V <sub>DDO_A</sub>   | Power  |                     | Output power supply for Bank QAx clock outputs.   |
| 31     | V <sub>DDO_A</sub>   | Power  |                     |   |

**Table 2. Pin Descriptions<sup>1</sup>** (Continued)

| Number | Name             | Type     |          | Description   |
|--------|------------------|----------|----------|---|
| 32     | QA1              | Output   |          | Single-ended output clocks, optimized at 125MHz. LVCMOS/LVTTL interface levels.   |
| 33     | QA0              | Output   |          |   |
| 34     | OE_A             | Input    | Pullup   | Output enable for Bank QAx outputs. The output bank is placed in a high-impedance mode on disable. LVCMOS/LVTTL interface levels.   |
| 35     | GND_QA           | Power    |          | Ground pin for Bank QAx clock outputs.  |
| 36     | GND              | Power    |          | Power supply ground.  |
| 37     | V <sub>DD</sub>  | Power    |          | Core supply pins.   |
| 38     | PSELB            | Input    | Pulldown | Select pin for Bank QBx first stage mux. Selects input for PLL enabled 25MHz (LOW) or phase detector input frequency (HIGH). LVCMOS/LVTTL interface levels.   |
| 39     | PLL_SELA         | Input    | Pullup   | Bypasses the PLL for Bank A outputs. When LOW, selects PLL (PLL Enable). When HIGH, bypasses the PLL. LVCMOS/LVTTL interface levels.  |
| 40     | PLL_SELB         | Input    | Pullup   | Select pin for Bank B second stage mux. Designed to operate with a phase detector input frequency of 25MHz. The Bank B outputs generate 125MHz when select pin is LOW and 25MHz when HIGH. LVCMOS/LVTTL interface levels. |
| 41     | GND_A            | Power    |          | Ground pin for PLL analog.  |
| 42     | V <sub>DDA</sub> | Power    |          | Analog supply pin.  |
| 43     | GND              | Power    |          | Power supply ground.  |
| 44     | V <sub>DD</sub>  | Power    |          | Core supply pins.   |
| 45     | RESERVED         | Reserved |          | Reserved pin. Do not connect.   |
| 46     | V <sub>DD</sub>  | Power    |          | Core supply pins.   |
| 47     | XTAL_SEL         | Input    | Pulldown | Select input for XTAL (LOW) or PCLK pre-divider (HIGH). LVCMOS/LVTTL interface levels.  |
| 48     | GND_XTAL         | Power    |          | Ground pin for XTAL.  |

NOTE 1: *Pullup* and *Pulldown* refer to internal input resistors. See [Table 2, Pin Characteristics](#), for typical values.

**Table 3. Pin Characteristics<sup>1</sup>**

| Symbol                | Parameter                                  |   | Test Conditions             | Minimum | Typical | Maximum | Units |
|-----------------------|--|---|-----------------------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance                          | PDIV_SEL, OE_REF, OE_A, OE_B, OE_C, PLL_SELA, PLL_SELB, PSELB, XTAL_SEL |                             |         | 3.5     |         | pF    |
| C <sub>PD</sub>       | Power Dissipation Capacitance (per output) |   | V <sub>DDO_X</sub> = 3.465V |         | 9       |         | pF    |
|                       |  |   | V <sub>DDO_X</sub> = 2.625V |         | 8       |         | pF    |
|                       |  |   | V <sub>DDO_X</sub> = 1.89V  |         | 5       |         | pF    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor                      |   |                             |         | 50      |         | kΩ    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor                    |   |                             |         | 50      |         | kΩ    |
| R <sub>OUT</sub>      | Output Impedance                           |   | V <sub>DDO_X</sub> = 3.3V   |         | 15      |         | Ω     |
|                       |  |   | V <sub>DDO_X</sub> = 2.5V   |         | 18      |         | Ω     |
|                       |  |   | V <sub>DDO_X</sub> = 1.8V   |         | 26      |         | Ω     |

NOTE 1: V<sub>DDO\_X</sub> denotes, V<sub>DDO\_A</sub>, V<sub>DDO\_B</sub>, V<sub>DDO\_C</sub>, V<sub>DDO\_REF</sub>.

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Electrical Characteristics* or *AC Electrical Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item                                     | Rating                               |
|--|--------------------------------------|
| Supply Voltage, $V_{DD}$                 | 3.63V                                |
| Inputs, $V_I$<br>XTAL_IN<br>Other Inputs | 0V to 2V<br>-0.5V to $V_{DD} + 0.5V$ |
| Outputs, $V_O$                           | -0.5V to $V_{DDO\_X} + 0.5V$         |
| Junction Temperature                     | 125°C                                |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C                       |

NOTE:  $V_{DDO\_X}$  denotes  $V_{DDO\_A}$ ,  $V_{DDO\_B}$ ,  $V_{DDO\_C}$  &  $V_{DDO\_REF}$ .

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = V_{DD\_XTAL} = V_{DDO\_X} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ <sup>1, 2</sup>**

| Symbol                  | Parameter                 | Test Conditions                        | Minimum         | Typical | Maximum  | Units |
|-------------------------|---------------------------|--|-----------------|---------|----------|-------|
| $V_{DD}$                | Core Supply Voltage       |  | 3.135           | 3.3     | 3.465    | V     |
| $V_{DD\_XTAL}$          | XTAL Power Supply Voltage |  | 3.135           | 3.3     | 3.465    | V     |
| $V_{DDA}$               | Analog Supply Voltage     |  | $V_{DD} - 0.06$ | 3.3     | $V_{DD}$ | V     |
| $V_{DDO\_X}$            | Output Supply Voltage     |  | 3.135           | 3.3     | 3.465    | V     |
| $I_{DD} + I_{DD\_XTAL}$ | Power Supply Current      |  |                 |         | 150      | mA    |
| $I_{DDA}$               | Analog Supply Current     |  |                 |         | 30       | mA    |
| $I_{DDO\_X}$            | Output Supply Current     | Outputs are Disabled to High-Impedance |                 |         | 8        | mA    |

NOTE 1:  $V_{DDO\_X}$  denotes,  $V_{DDO\_A}$ ,  $V_{DDO\_B}$ ,  $V_{DDO\_C}$ ,  $V_{DDO\_REF}$ .

NOTE 2:  $I_{DDO\_X}$  denotes,  $I_{DDO\_A} + I_{DDO\_B} + I_{DDO\_C} + I_{DDO\_REF}$ .

**Table 4B. Power Supply DC Characteristics,  $V_{DD} = V_{DD\_XTAL} = 3.3V \pm 5\%$ ,  $V_{DDO\_X} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ <sup>1, 2</sup>**

| Symbol                  | Parameter                 | Test Conditions                        | Minimum         | Typical | Maximum  | Units |
|-------------------------|---------------------------|--|-----------------|---------|----------|-------|
| $V_{DD}$                | Core Supply Voltage       |  | 3.135           | 3.3     | 3.465    | V     |
| $V_{DD\_XTAL}$          | XTAL Power Supply Voltage |  | 3.135           | 3.3     | 3.465    | V     |
| $V_{DDA}$               | Analog Supply Voltage     |  | $V_{DD} - 0.06$ | 3.3     | $V_{DD}$ | V     |
| $V_{DDO\_X}$            | Output Supply Voltage     |  | 2.375           | 2.5     | 2.625    | V     |
| $I_{DD} + I_{DD\_XTAL}$ | Power Supply Current      |  |                 |         | 150      | mA    |
| $I_{DDA}$               | Analog Supply Current     |  |                 |         | 30       | mA    |
| $I_{DDO\_X}$            | Output Supply Current     | Outputs are Disabled to High-Impedance |                 |         | 4        | mA    |

NOTE 1:  $V_{DDO\_X}$  denotes,  $V_{DDO\_A}$ ,  $V_{DDO\_B}$ ,  $V_{DDO\_C}$ ,  $V_{DDO\_REF}$ .

NOTE 2:  $I_{DDO\_X}$  denotes,  $I_{DDO\_A} + I_{DDO\_B} + I_{DDO\_C} + I_{DDO\_REF}$ .

**Table 4C. Power Supply DC Characteristics,  $V_{DD} = V_{DD\_XTAL} = 3.3V \pm 5\%$ ,  $V_{DDO\_X} = 1.8V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ <sup>1, 2</sup>**

| Symbol                  | Parameter                 | Test Conditions                        | Minimum         | Typical | Maximum  | Units |
|-------------------------|---------------------------|--|-----------------|---------|----------|-------|
| $V_{DD}$                | Core Supply Voltage       |  | 3.135           | 3.3     | 3.465    | V     |
| $V_{DD\_XTAL}$          | XTAL Power Supply Voltage |  | 3.135           | 3.3     | 3.465    | V     |
| $V_{DDA}$               | Analog Supply Voltage     |  | $V_{DD} - 0.06$ | 3.3     | $V_{DD}$ | V     |
| $V_{DDO\_X}$            | Output Supply Voltage     |  | 1.71            | 1.8     | 1.89     | V     |
| $I_{DD} + I_{DD\_XTAL}$ | Power Supply Current      |  |                 |         | 150      | mA    |
| $I_{DDA}$               | Analog Supply Current     |  |                 |         | 30       | mA    |
| $I_{DDO\_X}$            | Output Supply Current     | Outputs are Disabled to High-Impedance |                 |         | 3        | mA    |

NOTE 1:  $V_{DDO\_X}$  denotes,  $V_{DDO\_A}$ ,  $V_{DDO\_B}$ ,  $V_{DDO\_C}$ ,  $V_{DDO\_REF}$ .NOTE 2:  $I_{DDO\_X}$  denotes,  $I_{DDO\_A} + I_{DDO\_B} + I_{DDO\_C} + I_{DDO\_REF}$ .**Table 4D. Power Supply DC Characteristics,  $V_{DD} = V_{DD\_XTAL} = V_{DDO\_X} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ <sup>1, 2</sup>**

| Symbol                  | Parameter                 | Test Conditions                        | Minimum          | Typical | Maximum  | Units |
|-------------------------|---------------------------|--|------------------|---------|----------|-------|
| $V_{DD}$                | Core Supply Voltage       |  | 2.375            | 2.5     | 2.625    | V     |
| $V_{DD\_XTAL}$          | XTAL Power Supply Voltage |  | 2.375            | 2.5     | 2.625    | V     |
| $V_{DDA}$               | Analog Supply Voltage     |  | $V_{DD} - 0.054$ | 2.5     | $V_{DD}$ | V     |
| $V_{DDO\_X}$            | Output Supply Voltage     |  | 2.375            | 2.5     | 2.625    | V     |
| $I_{DD} + I_{DD\_XTAL}$ | Power Supply Current      |  |                  |         | 148      | mA    |
| $I_{DDA}$               | Analog Supply Current     |  |                  |         | 27       | mA    |
| $I_{DDO\_X}$            | Output Supply Current     | Outputs are Disabled to High-Impedance |                  |         | 4        | mA    |

NOTE 1:  $V_{DDO\_X}$  denotes,  $V_{DDO\_A}$ ,  $V_{DDO\_B}$ ,  $V_{DDO\_C}$ ,  $V_{DDO\_REF}$ .NOTE 2:  $I_{DDO\_X}$  denotes,  $I_{DDO\_A} + I_{DDO\_B} + I_{DDO\_C} + I_{DDO\_REF}$ .**Table 4E. Power Supply DC Characteristics,  $V_{DD} = V_{DD\_XTAL} = 2.5V \pm 5\%$ ,  $V_{DDO\_X} = 1.8V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ <sup>1, 2</sup>**

| Symbol                  | Parameter                 | Test Conditions                        | Minimum          | Typical | Maximum  | Units |
|-------------------------|---------------------------|--|------------------|---------|----------|-------|
| $V_{DD}$                | Core Supply Voltage       |  | 2.375            | 2.5     | 2.625    | V     |
| $V_{DD\_XTAL}$          | XTAL Power Supply Voltage |  | 2.375            | 2.5     | 2.625    | V     |
| $V_{DDA}$               | Analog Supply Voltage     |  | $V_{DD} - 0.054$ | 2.5     | $V_{DD}$ | V     |
| $V_{DDO\_X}$            | Output Supply Voltage     |  | 1.71             | 1.8     | 1.89     | V     |
| $I_{DD} + I_{DD\_XTAL}$ | Power Supply Current      |  |                  |         | 148      | mA    |
| $I_{DDA}$               | Analog Supply Current     |  |                  |         | 27       | mA    |
| $I_{DDO\_X}$            | Output Supply Current     | Outputs are Disabled to High-Impedance |                  |         | 3        | mA    |

NOTE 1:  $V_{DDO\_X}$  denotes,  $V_{DDO\_A}$ ,  $V_{DDO\_B}$ ,  $V_{DDO\_C}$ ,  $V_{DDO\_REF}$ .NOTE 2:  $I_{DDO\_X}$  denotes,  $I_{DDO\_A} + I_{DDO\_B} + I_{DDO\_C} + I_{DDO\_REF}$ .

**Table 4F. LVCMOS/LVTTL DC Characteristics,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ <sup>1</sup>**

| Symbol   | Parameter           |  | Test Conditions   | Minimum | Typical | Maximum        | Units         |
|----------|---------------------|--|---|---------|---------|----------------|---------------|
| $V_{IH}$ | Input High Voltage  |  | $V_{DD} = 3.3\text{V} \pm 5\%$  | 2       |         | $V_{DD} + 0.3$ | V             |
|          |                     |  | $V_{DD} = 2.5\text{V} \pm 5\%$  | 1.7     |         | $V_{DD} + 0.3$ | V             |
| $V_{IL}$ | Input Low Voltage   |  | $V_{DD} = 3.3\text{V} \pm 5\%$  | -0.3    |         | 0.8            | V             |
|          |                     |  | $V_{DD} = 2.5\text{V} \pm 5\%$  | -0.3    |         | 0.7            | V             |
| $I_{IH}$ | Input High Current  | PSELB, XTAL_SEL, PDIV_SEL                    | $V_{DD} = V_{IN} = 3.465\text{V}$ or $2.625\text{V}$                  |         |         | 150            | $\mu\text{A}$ |
|          |                     | OE_REF, PLL_SELA, PLL_SELB, OE_A, OE_B, OE_C | $V_{DD} = V_{IN} = 3.465\text{V}$ or $2.625\text{V}$                  |         |         | 5              | $\mu\text{A}$ |
| $I_{IL}$ | Input Low Current   | PSELB, XTAL_SEL, PDIV_SEL                    | $V_{DD} = 3.465\text{V}$ or $2.625\text{V}$ ,<br>$V_{IN} = 0\text{V}$ | -5      |         |                | $\mu\text{A}$ |
|          |                     | OE_REF, PLL_SELA, PLL_SELB, OE_A, OE_B, OE_C | $V_{DD} = 3.465\text{V}$ or $2.625\text{V}$ ,<br>$V_{IN} = 0\text{V}$ | -150    |         |                | $\mu\text{A}$ |
| $V_{OH}$ | Output High Voltage |  | $V_{DDO\_X} = 3.3\text{V} \pm 5\%$ ; $I_{OH} = -12\text{mA}$          | 2.6     |         |                | V             |
|          |                     |  | $V_{DDO\_X} = 2.5\text{V} \pm 5\%$ ; $I_{OH} = -12\text{mA}$          | 1.8     |         |                | V             |
|          |                     |  | $V_{DDO\_X} = 1.8\text{V} \pm 5\%$ ; $I_{OH} = -8\text{mA}$           | 1.3     |         |                | V             |
| $V_{OL}$ | Output Low Voltage; |  | $V_{DDO\_X} = 3.3\text{V} \pm 5\%$ , $I_{OL} = 12\text{mA}$           |         |         | 0.5            | V             |
|          |                     |  | $V_{DDO\_X} = 2.5\text{V} \pm 5\%$ , $I_{OL} = 12\text{mA}$           |         |         | 0.5            | V             |
|          |                     |  | $V_{DDO\_X} = 1.8\text{V} \pm 5\%$ , $I_{OL} = 8\text{mA}$            |         |         | 0.4            | V             |

 NOTE 1:  $V_{DDO\_X}$  denotes,  $V_{DDO\_A}$ ,  $V_{DDO\_B}$ ,  $V_{DDO\_C}$ ,  $V_{DDO\_REF}$ .

**Table 4G. LVPECL Differential DC Characteristics,  $V_{DD} = 3.3\text{V} \pm 5\%$  or  $2.5\text{V} \pm 5\%$ ,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$** 

| Symbol    | Parameter                                |             | Test Conditions   | Minimum   | Typical | Maximum  | Units         |
|-----------|--|-------------|---|-----------|---------|----------|---------------|
| $I_{IH}$  | Input High Current                       | PCLK, nPCLK | $V_{DD} = V_{IN} = 3.465\text{V}$ or $2.625\text{V}$                  |           |         | 150      | $\mu\text{A}$ |
| $I_{IL}$  | Input Low Current                        | PCLK        | $V_{DD} = 3.465\text{V}$ or $2.625\text{V}$ ,<br>$V_{IN} = 0\text{V}$ | -5        |         |          | $\mu\text{A}$ |
|           |  | nPCLK       | $V_{DD} = 3.465\text{V}$ or $2.625\text{V}$ ,<br>$V_{IN} = 0\text{V}$ | -150      |         |          | $\mu\text{A}$ |
| $V_{PP}$  | Peak-to-Peak Voltage <sup>1</sup>        |             |   | 0.3       |         | 1.0      | V             |
| $V_{CMR}$ | Common Mode Input Voltage <sup>1,2</sup> |             |   | GND + 1.5 |         | $V_{DD}$ | V             |

 NOTE 1:  $V_{IL}$  should not be less than  $-0.3\text{V}$  and  $V_{IH}$  should not be greater than  $V_{DD}$ .

NOTE 2: Common mode voltage is defined at the crosspoint.

**Table 5. Input Frequency Characteristics,  $V_{DD} = V_{DD\_XTAL} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

| Symbol   | Parameter       | Test Conditions   | Minimum      | Typical | Maximum | Units |     |
|----------|-----------------|-------------------|--------------|---------|---------|-------|-----|
| $f_{IN}$ | Input Frequency | XTAL_IN, XTAL_OUT |              | 25      |         | MHz   |     |
|          |                 | PCLK, nPCLK       | PDIV_SEL = 0 |         | 25      |       | MHz |
|          |                 |                   | PDIV_SEL = 1 |         | 125     |       | MHz |

**Table 6. Crystal Characteristics<sup>1</sup>**

| Parameter                          | Test Conditions | Minimum     | Typical | Maximum | Units    |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation                |                 | Fundamental |         |         |          |
| Frequency                          |                 |             | 25      |         | MHz      |
| Load Capacitance ( $C_L$ )         |                 |             | 12      | 18      | pF       |
| Equivalent Series Resistance (ESR) |                 |             |         | 50      | $\Omega$ |
| Shunt Capacitance                  |                 |             |         | 7       | pF       |

NOTE 1: IDT Part#603-25-173 recommended.



## AC Electrical Characteristics

**Table 7. AC Characteristics,**  $V_{DD} = V_{DD\_XTAL} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{DDO\_A}, V_{DDO\_B}, V_{DDO\_C}, V_{DDO\_REF} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$  or  $1.8V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$ <sup>1</sup>

| Symbol               | Parameter   | Test Conditions         |         | Minimum | Typical | Maximum | Units |
|----------------------|---|-------------------------|---------|---------|---------|---------|-------|
| $f_{OUT}$            | Output Frequency  | PLL Mode                |         | 24      |         | 125     | MHz   |
| tsk(o)               | Output Skew <sup>2, 3</sup>   | $f_{OUT} = 125MHz$      |         |         |         | 120     | ps    |
| tsk(b)               | Bank Skew <sup>2, 4</sup>   | $f_{OUT} = 125MHz$      |         |         |         | 50      | ps    |
| $f_{jit}(\emptyset)$ | Phase Jitter, RMS;<br>Integration Range:<br>12kHz – 20MHz <sup>5, 6</sup> | VDDO = 3.3V             | QA[0:4] |         | 0.60    |         | ps    |
|                      |   |                         | QB[0:2] |         | 1.20    |         | ps    |
|                      |   | VDDO = 2.5V             | QA[0:4] |         | 0.45    |         | ps    |
|                      |   |                         | QB[0:2] |         | 0.93    |         | ps    |
|                      |   | VDDO = 1.8V             | QA[0:4] |         | 0.40    |         | ps    |
|                      |   |                         | QB[0:2] |         | 0.76    |         | ps    |
| $f_{jit}(cc)$        | Cycle-to-Cycle Jitter <sup>2, 5</sup>                                     | $f_{OUT} = 125MHz$      |         |         | 20      | 45      | ps    |
| $f_{jit}(per)$       | RMS Period Jitter <sup>2, 5</sup>   | $f_{OUT} = 125MHz$      |         |         | 3       | 6       | ps    |
| $t_L$                | PLL Lock Time   |                         |         |         | 13      |         | ms    |
| odc                  | Output Duty Cycle   | PLL Mode (QAx, QBx, QC) |         | 45      |         | 55      | %     |
| $t_R / t_F$          | Output Rise/Fall Time   | 20% to 80%              |         |         |         | 900     | ps    |

NOTE 1: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

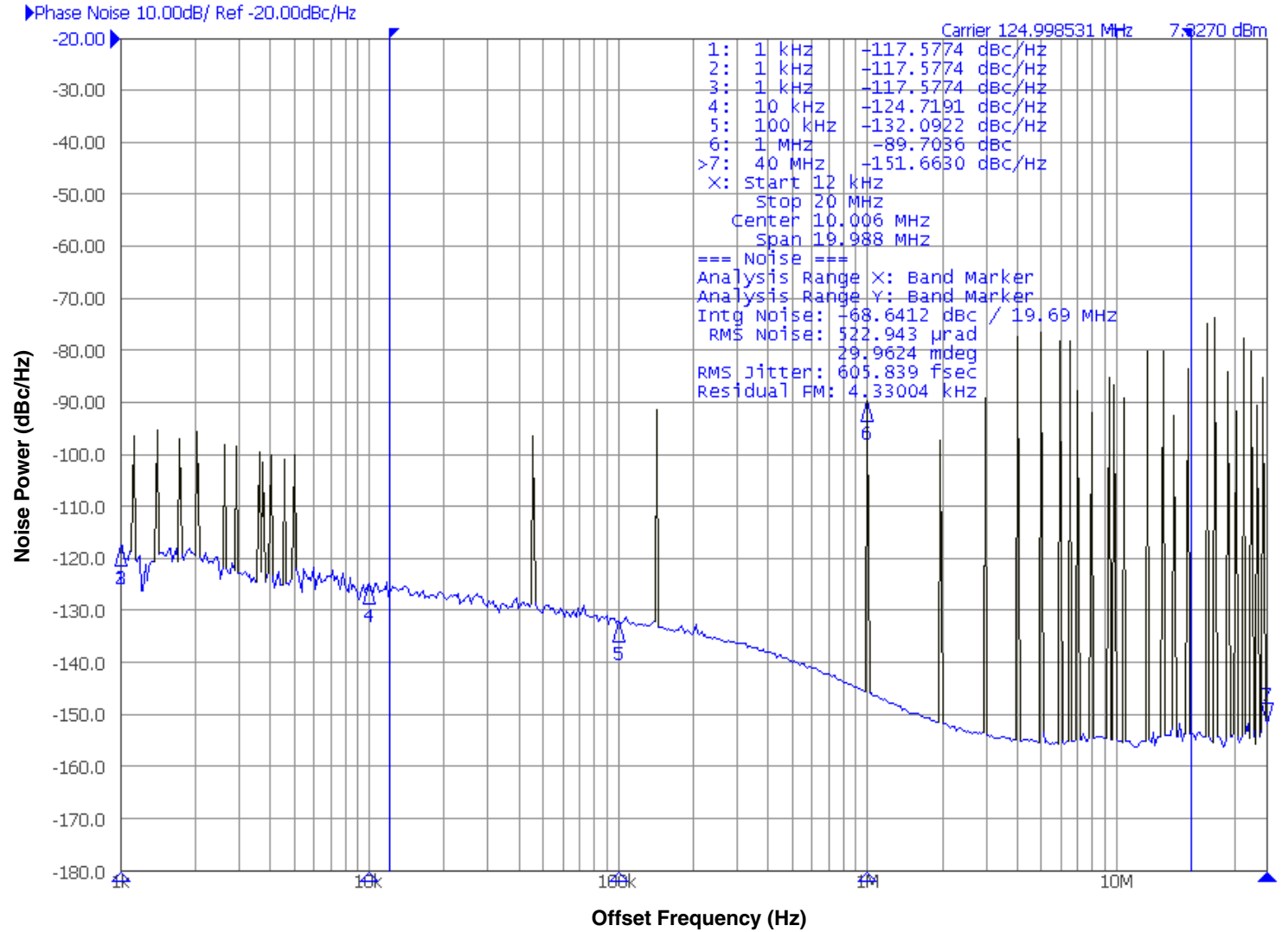
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.

NOTE 4: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.

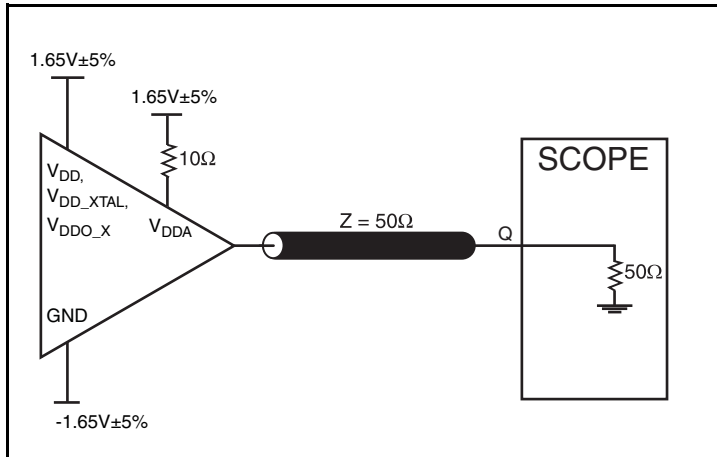
NOTE 5: Jitter performance using XTAL inputs.

NOTE 6: Measured with Bank A at 125MHz, Bank B at 125MHz, QC and QREF enabled.

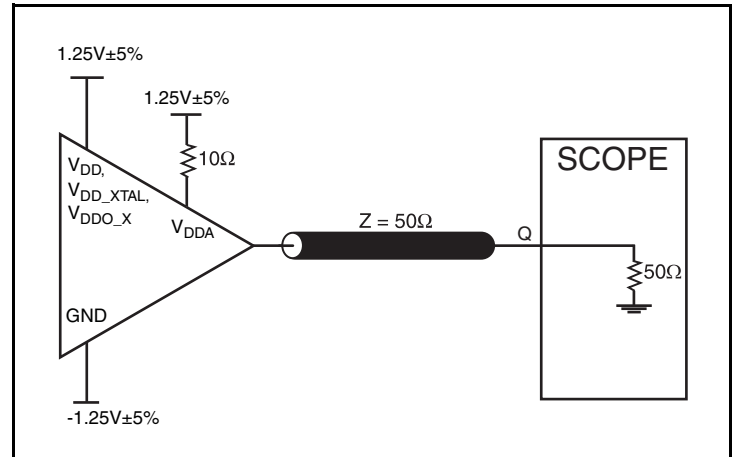
### Typical Phase Noise at 125MHz



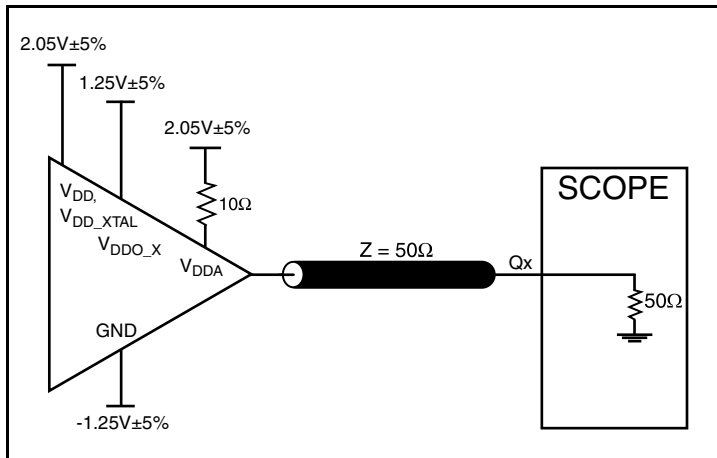
Parameter Measurement Information



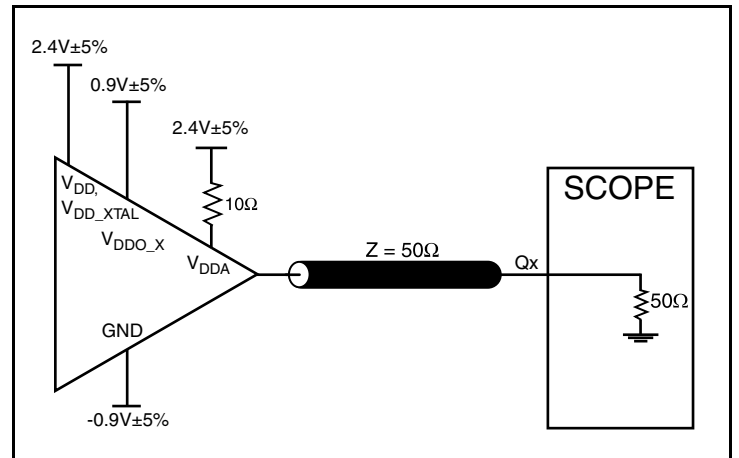
3.3V Core/3.3V LVCMOS Output Load Test Circuit



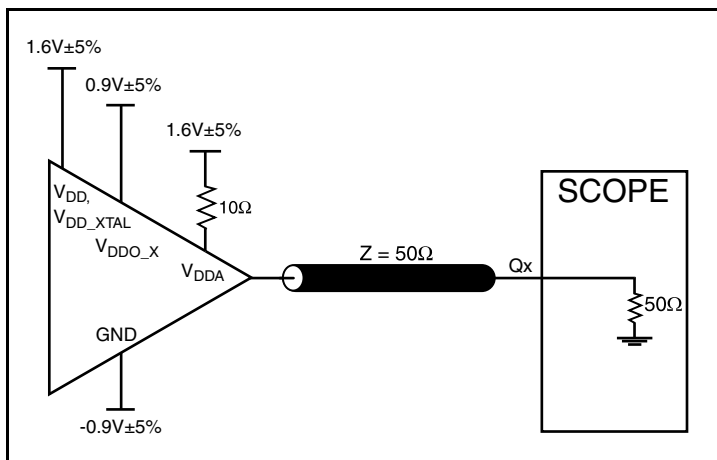
2.5V Core/2.5V LVCMOS Output Load Test Circuit



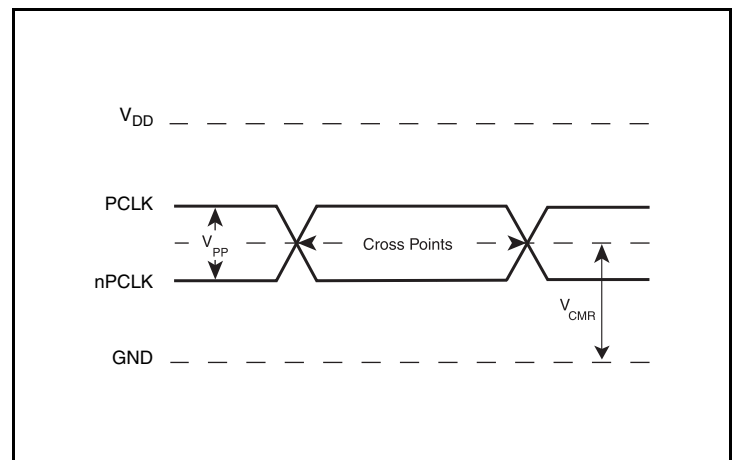
3.3V Core/2.5V LVCMOS Output Load Test Circuit



3.3V Core/1.8V LVCMOS Output Load Test Circuit

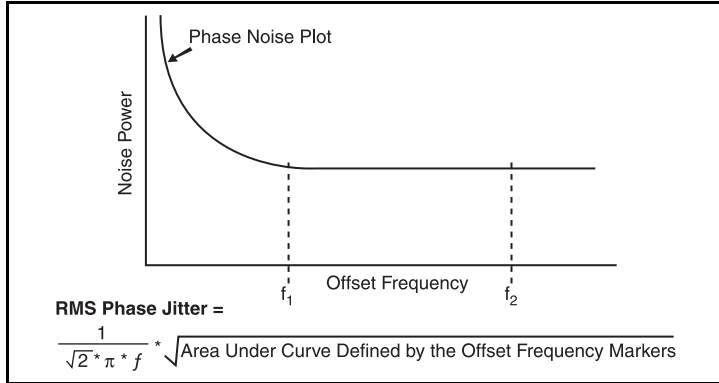


2.5V Core/1.8V LVCMOS Output Load Test Circuit

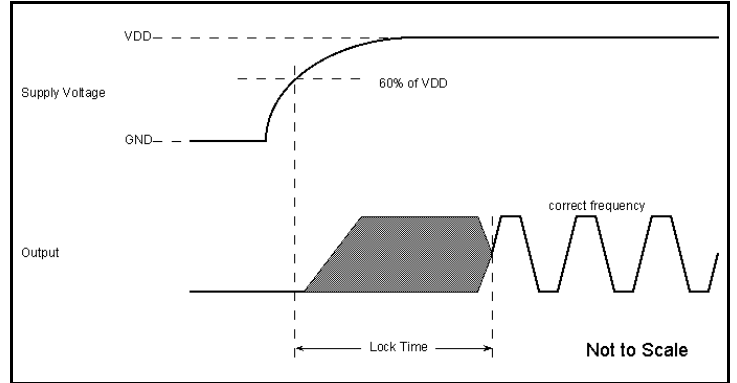


Differential Input Level

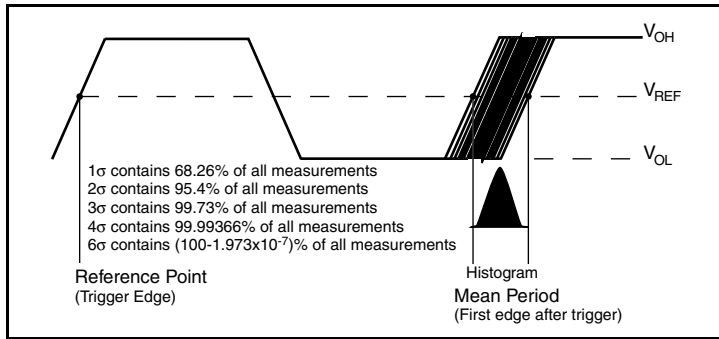
## Parameter Measurement Information, continued



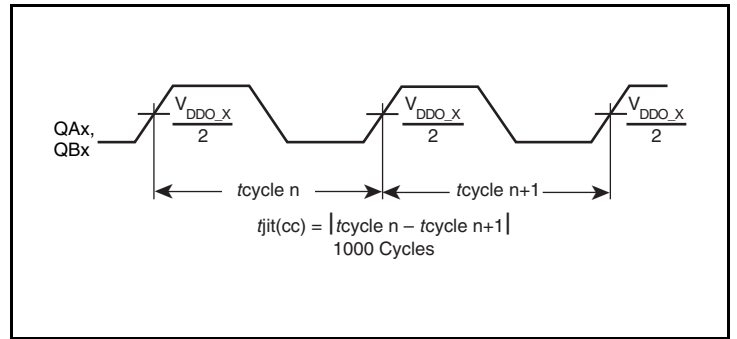
**RMS Phase Jitter**



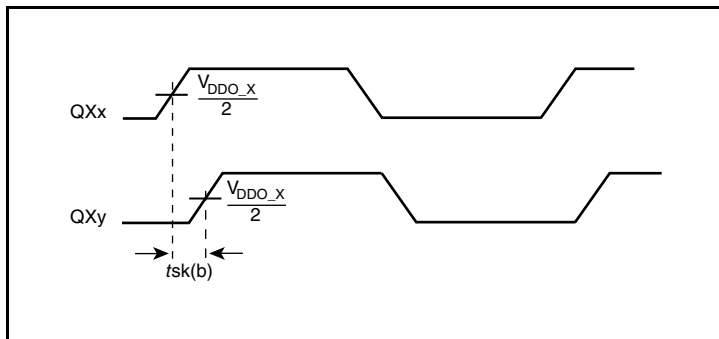
**PLL Lock Time**



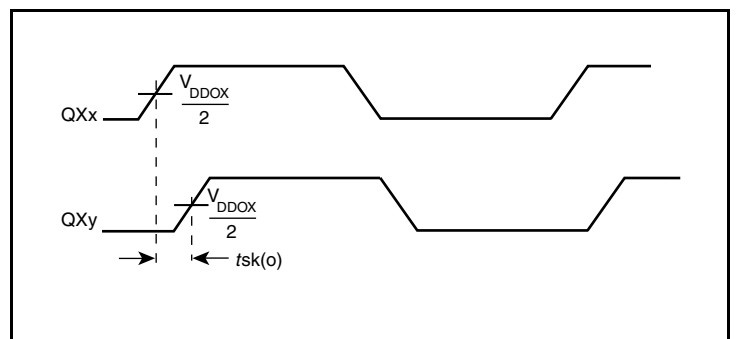
**RMS Period Jitter**



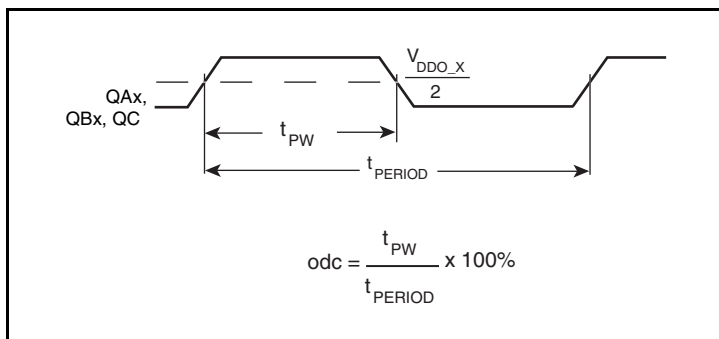
**Cycle-to-Cycle Jitter**



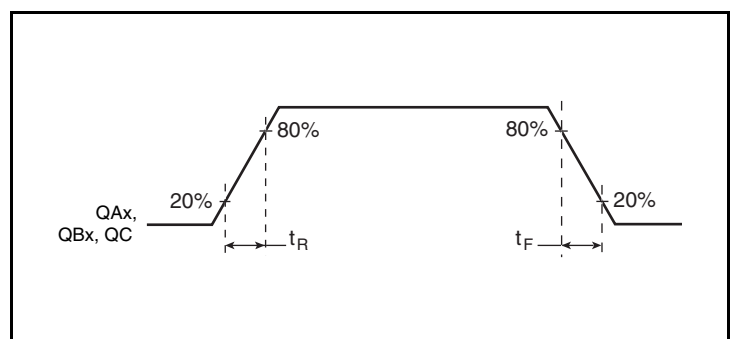
**Bank Skew**



**Output Skew**



**Output Duty Cycle/Pulse Width/Period**



**Output Rise Fall Time**

## Applications Information

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### LVC MOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

##### PCLK/nPCLK Inputs

For applications not requiring the use of the differential input, both PCLK and nPCLK can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from PCLK to ground.

##### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from XTAL\_IN to ground.

#### Outputs:

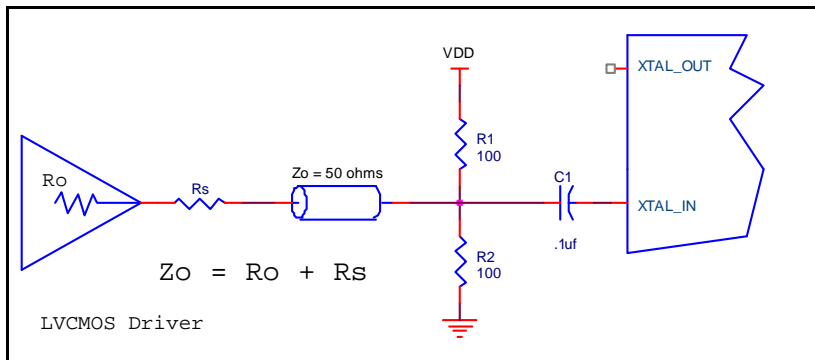
##### LVC MOS Outputs

All unused LVC MOS outputs can be left floating. There should be no trace attached.

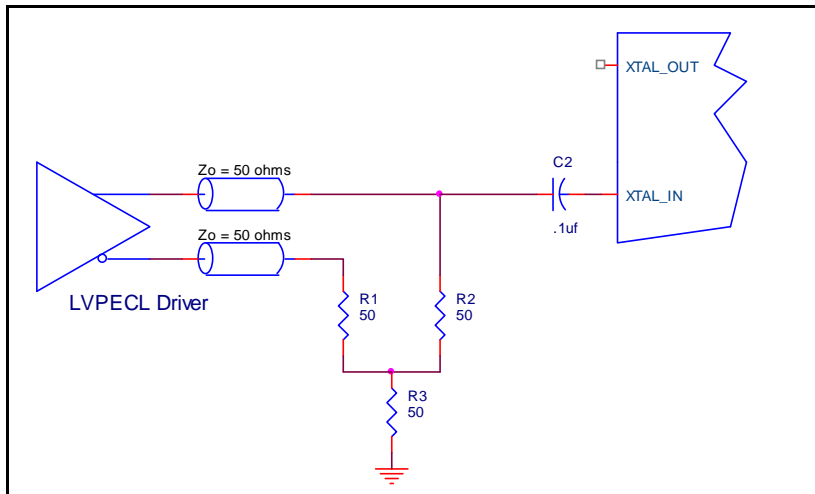
## Overdriving the XTAL Interface

The XTAL\_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL\_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. [Figure 1A](#) shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This

can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and changing  $R_2$  to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. [Figure 1B](#) shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL\_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.



**Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface**

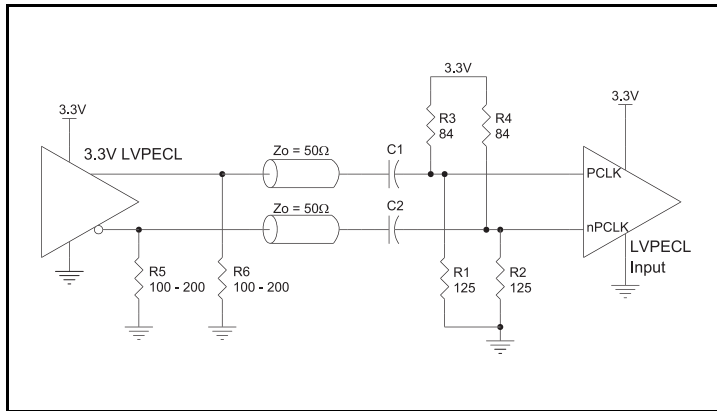


**Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface**

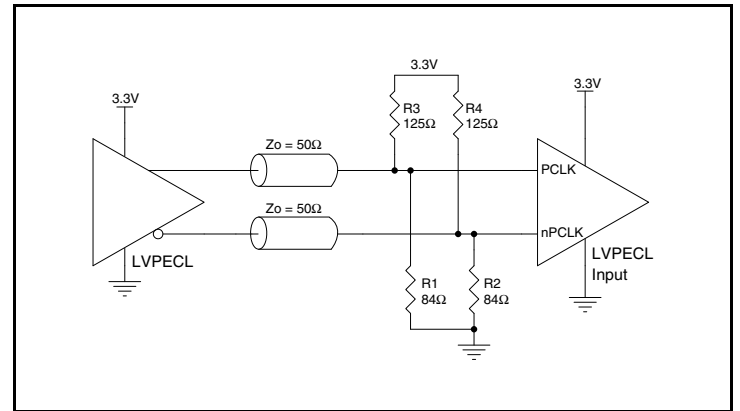
### 3.3V LVPECL Clock Input Interface

The PCLK/nPCLK accepts LVPECL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. [Figure 2A](#) to [Figure 2B](#) show interface examples for the PCLK/nPCLK input driven by the most common driver types. The

input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



**Figure 2A. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple**

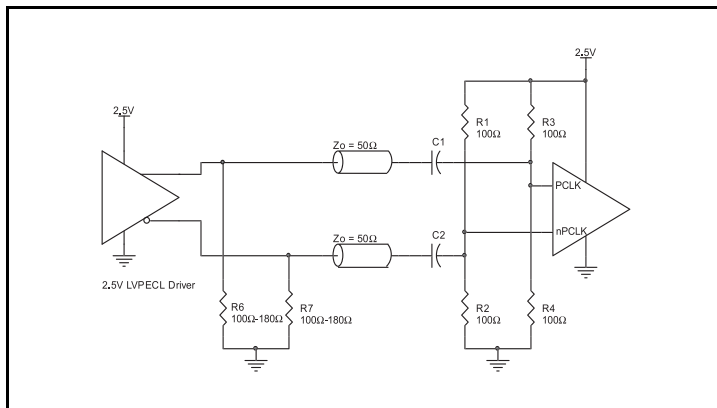


**Figure 2B. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver**

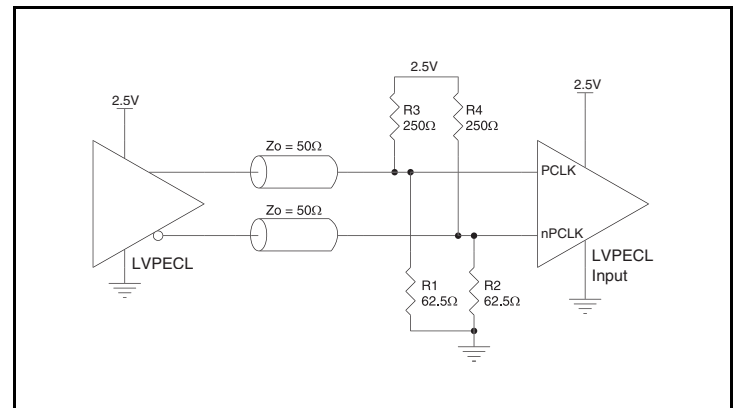
### 2.5V LVPECL Clock Input Interface

The PCLK/nPCLK accepts LVPECL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. [Figure 3A](#) to [Figure 3B](#) show interface examples for the PCLK/nPCLK input driven by the most common driver types. The

input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



**Figure 3A. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver with AC Couple**



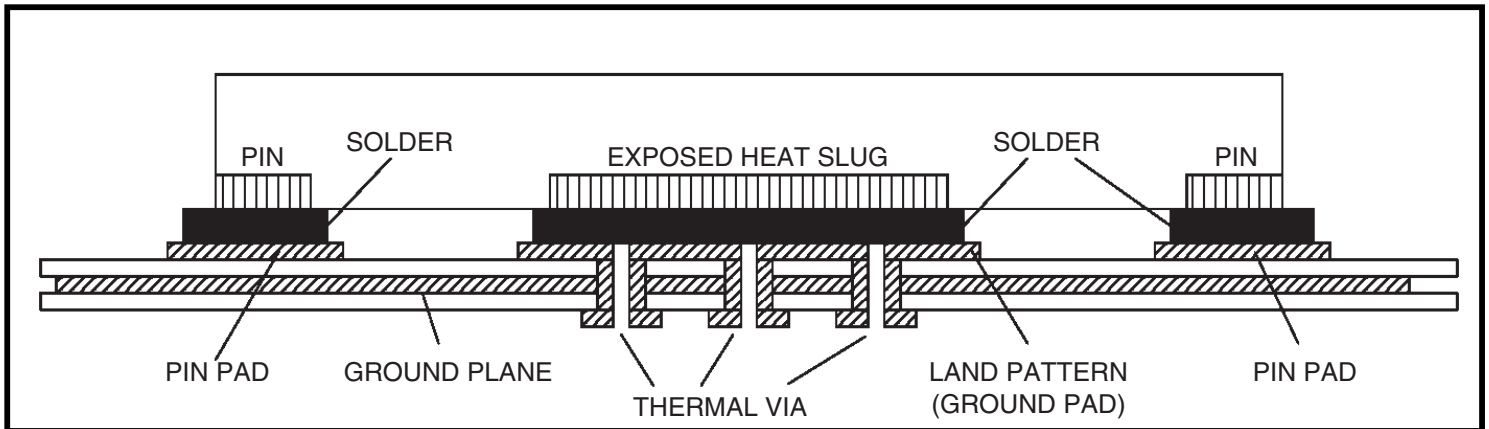
**Figure 3B. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver**

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in [Figure 4](#). The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.



**Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**



## Schematic Example

*Figure 5* (next page) shows an example 840NT4-01 application schematic. This schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set. In this schematic, the device is operated at  $V_{DD} = V_{DDA} = 2.5V$  and  $V_{DDO\_A}$ ,  $V_{DDO\_B}$ ,  $V_{DDO\_C}$  and  $V_{DDO\_REF} = 1.8V$ .

A 12pF parallel resonant 25MHz crystal (IDT/ Fox Part #603-25-173) is used with the recommended load capacitors  $C1 = C2 = 3.3pF$  for frequency accuracy. Depending on the parasitic capacity on the crystal terminals of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will require adjusting C1 and C2. For this device, the crystal load capacitors are required for proper operation.

Crystal layout is very important to minimize capacitive coupling between the crystal pads and leads and other metal in the circuit board. Capacitive coupling to other conductors has two adverse effects; it reduces the oscillator frequency leaving less tuning margin and noise coupling from power planes and logic transitions on signal traces can pull the phase of the crystal resonance, inducing jitter. Routing I<sup>2</sup>C under the crystal is a very common layout error, based on the assumption that it is a low frequency signal and will not affect the crystal oscillation. In fact, I<sup>2</sup>C transition times are short enough to capacitively couple into the crystal if they are routed close enough to the crystal traces.

In layout, all capacitive coupling to the crystal from any signal trace is to be minimized, that is to the XTAL\_IN and XTAL\_OUT pins, traces to the crystal pads, the crystal pads and the tuning capacitors. Using a crystal on the top layer as an example, void all signal and power layers under the crystal connections between the top layer and the ground plane used by the 840NT4-01. Then calculate the parasitic capacity to the ground and determine if it is large enough to preclude tuning the oscillator. If the coupling is excessive, particularly if the first layer under the crystal is a ground plane, a layout option is to void the

ground plane and all deeper layers until the next ground plane is reached. The ground connection of the tuning capacitors should first be made between the capacitors on the top layer, then a single ground via is dropped to connect the tuning cap ground to the ground plane as close to the 840NT4-01 as possible as shown in the schematic.

This device package has an ePAD that is connected to ground internally. The ePAD is to be connected to  $V_{EE}/GND$  through vias in order to improve heat dissipation.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 840NT4-01 provides separate power supply pins to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1 $\mu$ F capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

For additional layout recommendations and guidelines, contact [clocks@idt.com](mailto:clocks@idt.com).

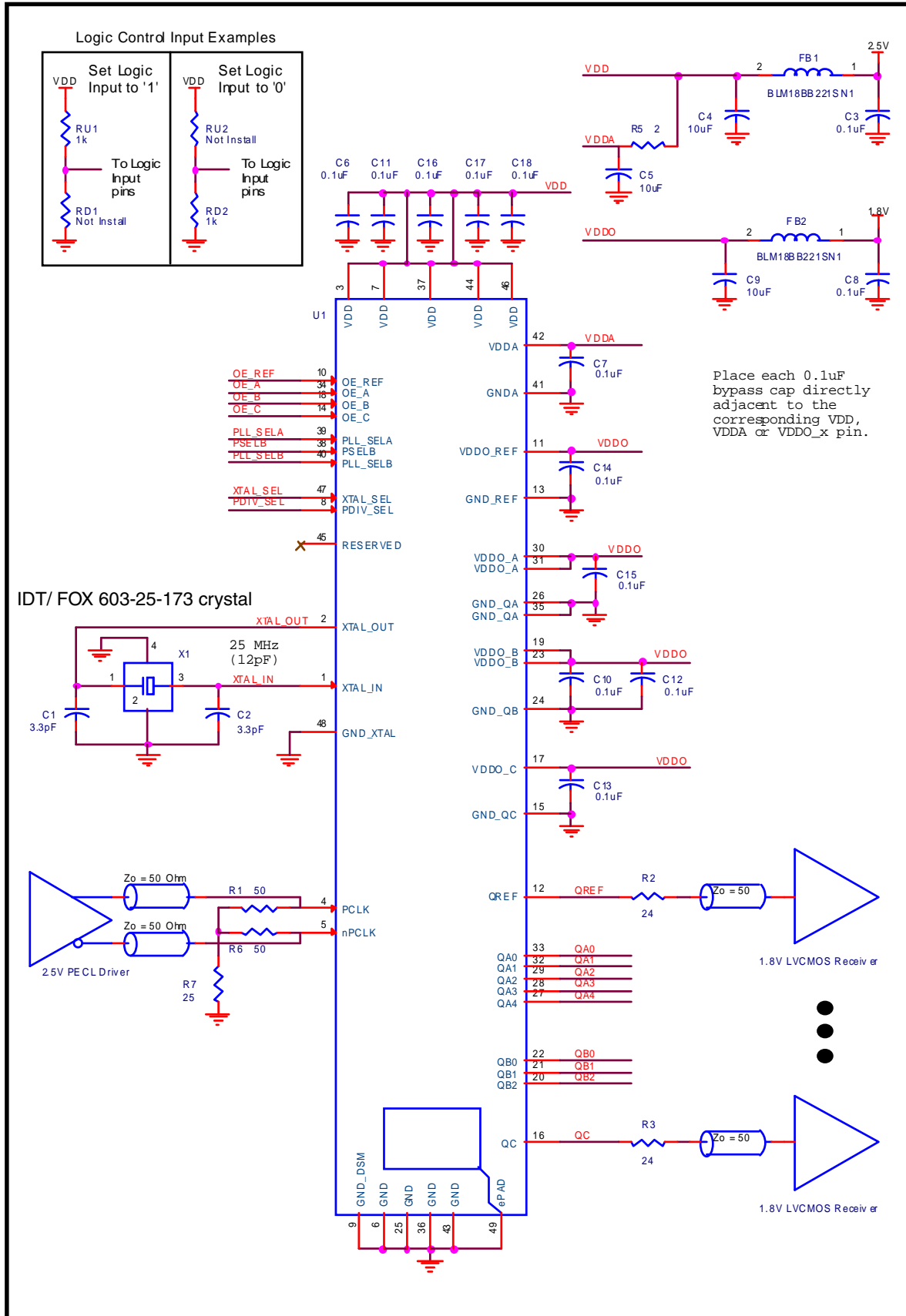


Figure 5. 840NT4-01 Schematic Layout

## Power Considerations

This section provides information on power dissipation and junction temperature for the 840NT4-01. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 840NT4-01 is the sum of the static power plus the dynamic power dissipation due to loading. The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

The maximum core current at 85°C,  $I_{DDmax} = 150mA$

Static Power (max)

$$\begin{aligned}
 &= [V_{DD\_MAX} * (I_{DD\_MAX} + I_{DD\_XTAL} + I_{DDA} + I_{DDO\_X})] \\
 &= [3.465V * (150mA + 30mA + 8mA)] \\
 &= \mathbf{651.4mW}
 \end{aligned}$$

Dynamic Power Dissipation (max), Clocks for Freescale B4/T4 Processor

$$\begin{aligned}
 &= [C_{PD} * (N * Frequency + N * Frequency + N * Frequency) * (V_{DDO})^2] \\
 &= [9pF * (8 * 125MHz + 1 * 25MHz + 1 * 24MHz) * (3.465V)^2] \\
 &= \mathbf{113.4mW}
 \end{aligned}$$

### Total Power

$$\begin{aligned}
 &= \text{Static Power} + \text{Dynamic Power Dissipation} \\
 &= 651.4mW + 113.4mW \\
 &= \mathbf{0.765W}
 \end{aligned}$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd_{total} + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd_{total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 30°C/W per [Table 8](#) below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.765\text{W} * 30^\circ\text{C/W} = 108^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 8. Thermal Resistance  $\theta_{JA}$  for a 48-lead VFQFN Package**

| Meters per Second                           | $\theta_{JA}$ by Velocity |          |          |
|---|---------------------------|----------|----------|
|   | 0                         | 1        | 2        |
| Multi-Layer PCB, JEDEC Standard Test Boards | 30°C/W                    | 23.1°C/W | 19.8°C/W |

## Reliability Information

**Table 9.  $\theta_{JA}$  vs. Air Flow Table for a 48-Lead VFQFN**

| $\theta_{JA}$ by Velocity                   |        |          |          |
|---|--------|----------|----------|
| Meters per Second                           | 0      | 1        | 2        |
| Multi-Layer PCB, JEDEC Standard Test Boards | 30°C/W | 23.1°C/W | 19.8°C/W |

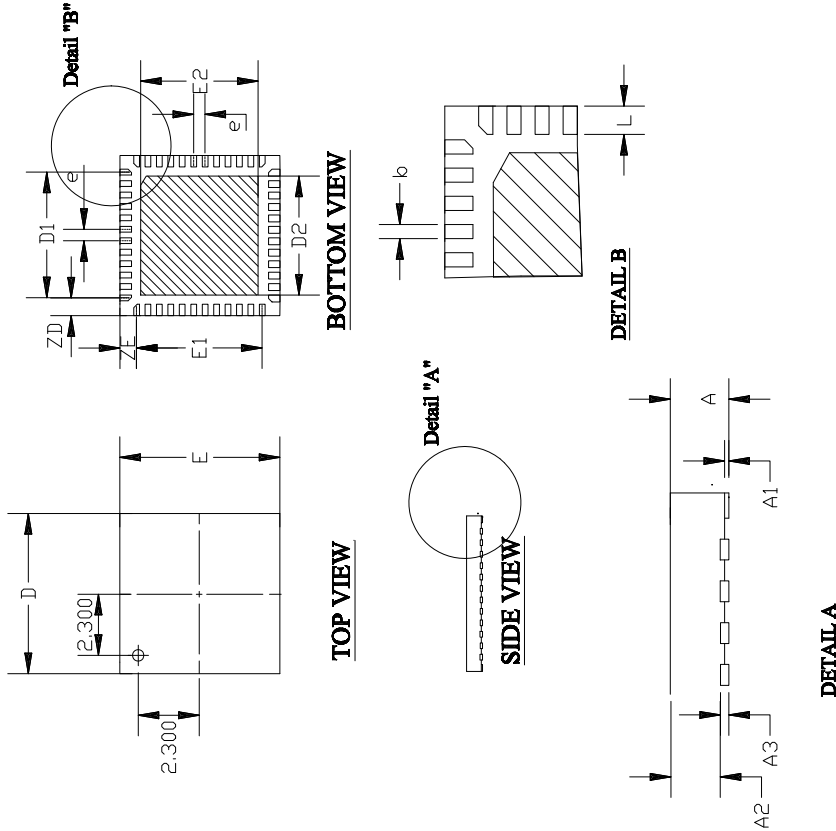
## Transistor Count

The transistor count for 840NT4-01 is: 24,508

# 48-Lead VFQFN Package Outline and Package Dimensions

| REVISIONS |     |                   |          |          |
|-----------|-----|-------------------|----------|----------|
| DCN       | REV | DESCRIPTION       | DATE     | APPROVED |
|           | 00  | INITIAL RELEASE   | 10/18/07 |          |
|           | 01  | Change Dim on "A" | 07/07/09 | MA       |

**FOR REFERENCE ONLY**



| Symbol | Dimension in mm |      |      |
|--------|-----------------|------|------|
|        | Min             | Nom  | Max  |
| A      | —               | 0.8  | 0.9  |
| A1     | 0.00            | 0.02 | 0.05 |
| A3     | 0.2 REF         |      |      |
| b      | 0.18            | 0.25 | 0.3  |
| D      | 7.00 BSC        |      |      |
| D1     | 5.50 BSC        |      |      |
| E      | 7.00 BSC        |      |      |
| E1     | 5.50 BSC        |      |      |
| e      | 0.50 BSC        |      |      |
| R      | 0.20~0.25       |      |      |
| N      | 48              |      |      |
| L      | 0.35            | 0.40 | 0.45 |
| E2     | 5.50            | 5.65 | 5.80 |
| D2     | 5.50            | 5.65 | 5.80 |
| ZD     | 0.75 BSC        |      |      |
| ZE     | 0.75 BSC        |      |      |

|  |         |         |      |       |         |           |      |       |      |  |          |              |
|--|---------|---------|------|-------|---------|-----------|------|-------|------|--|----------|--------------|
| TOLERANCES<br>UNLESS SPECIFIED   | DECIMAL | ANGULAR | DATE | DRAWN | CHECKED | APPROVALS | DATE | TITLE | SIZE | DRAWING No.  | REV      | SHEET        |
|  | XXX.X   | ±       |      |       |         |           |      |       |      |  |          |              |
|  | XXX.X   | ±       |      |       |         |           |      |       |      |  |          |              |
|  | XXX.X   | ±       |      |       |         |           |      |       |      |  |          |              |
| IDT 6024 Silver Creek Valley Road<br>San Jose, CA 95138<br>PHONE: (408) 284-8200<br>FAX: (408) 284-8591<br>www.IDT.com |         |         |      |       |         |           |      |       |      | NL/NLG 48 PACKAGE OUTLINE<br>7.0 X 7.0 mm BODY<br>0.5 mm PITCH QFN |          |              |
|  |         |         |      |       |         |           |      |       |      | C  | PSC-4203 | 01           |
|  |         |         |      |       |         |           |      |       |      | DO NOT SCALE DRAWING   |          | SHEET 1 OF 1 |

**48L QFN 7x7**

**DETAIL A**

**DETAIL B**

**TOP VIEW**

**BOTTOM VIEW**

**SIDE VIEW**

**Detail "A"**

**Detail "B"**

## Ordering Information

**Table 10. Ordering Information**

| <b>Part/Order Number</b> | <b>Marking</b>   | <b>Package</b>           | <b>Shipping Packaging</b> | <b>Temperature</b> |
|--------------------------|------------------|--------------------------|---------------------------|--------------------|
| 840NT4-01NLGI            | IDT840NT4-01NLGI | 48-Lead VFQFN, Lead-Free | Tray                      | -40°C to 85°C      |
| 840NT4-01NLGI8           | IDT840NT4-01NLGI | 48-Lead VFQFN, Lead-Free | Tape & Reel               | -40°C to 85°C      |

## Revision History Sheet

| Rev | Table | Page | Description of Change   | Date    |
|-----|-------|------|---|---------|
| 2   |       | 8    | <i>Crystal Characteristics</i> - added note.                      | 5/18/15 |
|     |       | 17   | <i>Schematic Example</i> - revised first sentence of paragraph 2. |         |
|     |       | 18   | <i>840NT4-01 Schematic Layout</i> - revised crystal note.         |         |
|     |       |      |   |         |
|     |       |      |   |         |



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