Programmable FemtoClock® NG LVPECL/LVDS Clock Generator with 8-Outputs

IDT8T49N008I

DATASHEET

General Description

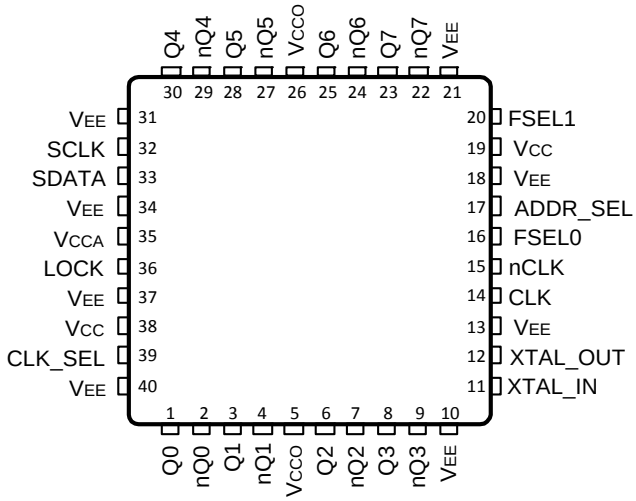
The IDT8T49N008I is an eight output Clock Synthesizer with selectable LVDS or LVPECL outputs. The IDT8T49N008I can synthesize any one of four frequencies from a single crystal or reference clock. The four frequencies are selected from the Frequency Selection Table (Table 3A) and are programmed via I^2C interface. The four predefined frequencies are selected in the user application by two frequency selection pins. Note the desired programmed frequencies must be used with the corresponding crystal or clock frequency as indicated in Table 3A.

Excellent phase noise performance is maintained with IDT's Fourth Generation FemtoClock® NG PLL technology, which delivers sub-400fs RMS phase jitter.

Features

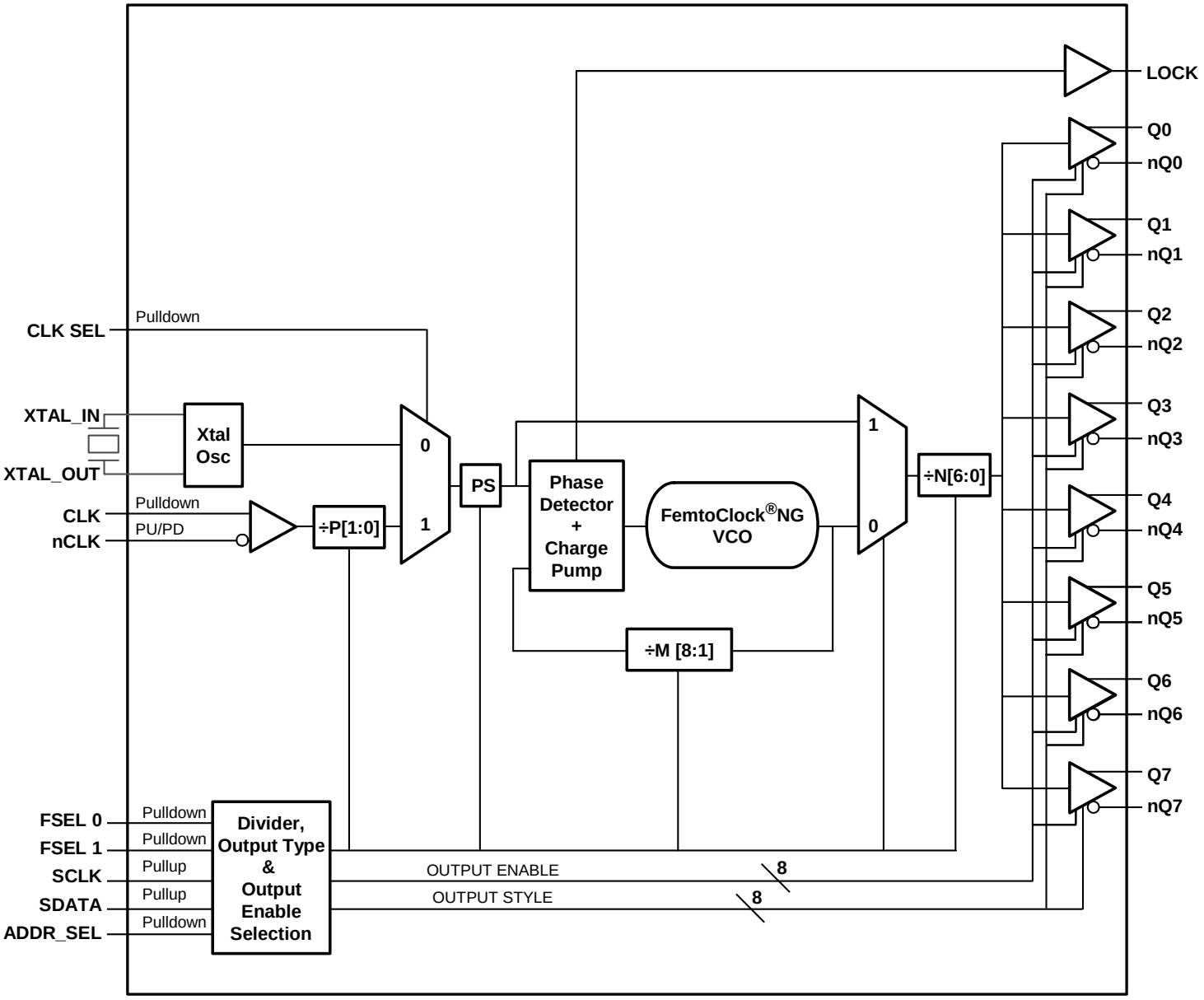
- Fourth Generation FemtoClock NG PLL technology
- Eight selectable LVPECL or LVDS outputs
- CLK, nCLK input pair can accept the following differential input levels: LVPECL, LVDS, HCSL
- FemtoClock NG VCO Range: 1.91GHz - 2.5GHz
- RMS phase jitter at 156.25MHz (12kHz - 20MHz): 228fs (typical)
- RMS phase jitter at 156.25MHz (10kHz - 1MHz): 175fs (typical)
- Full 2.5V or 3.3V power supply
- I^2C programming interface
- PCI Express (2.5 Gb/S), Gen 2 (5 Gb/s) and Gen 3 (8 Gb/s) jitter compliant
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

Pin Assignment



IDT8T49N008I
40-Lead VFQFN
6mm x 6mm x 0.925mm package body
4.65mm x 4.65mm E-Pad
NL Package

Block Diagram



Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVPECL or LVDS interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. LVPECL or LVDS interface levels.
5, 26	V_{CCO}	Power		Output supply pins.
6, 7	Q2, nQ2	Output		Differential output pair. LVPECL or LVDS interface levels.
8, 9	Q3, nQ3	Output		Differential output pair. LVPECL or LVDS interface levels.
10, 13, 18, 21, 31, 34, 37, 40	V_{EE}	Power		Negative supply pins.
11, 12	XTAL_IN XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output. Crystal frequency is selected from Table 3A.
14	CLK	Input	Pulldown	Non-inverting differential clock input.
15	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. Internal resistor bias to $V_{CC}/2$.
16, 20	FSEL0, FSEL1	Input	Pulldown	Frequency and configuration. Selects between one of four factory programmable power-up default configurations. The four configurations can have different PLL states, output frequencies, output styles and output states. These default configurations can be overwritten after power-up via I^2C. LVCMOS/LVTTL interface levels. 00 = Configuration 0 (default) 01 = Configuration 1 10 = Configuration 2 11 = Configuration 3
17	ADDR_SEL	Input	Pulldown	I^2C Address select pin. LVCMOS/LVTTL interface levels.
19, 38	V_{CC}	Power		Core supply pins.
22, 23	nQ7, Q7	Output		Differential output pair. LVPECL or LVDS interface levels.
24, 25	nQ6, Q6	Output		Differential output pair. LVPECL or LVDS interface levels.
27, 28	nQ5, Q5	Output		Differential output pair. LVPECL or LVDS interface levels.
29, 30	nQ4, Q4	Output		Differential output pair. LVPECL or LVDS interface levels.
32	SCLK	Input	Pullup	I^2C Clock Input. LVCMOS/LVTTL interface levels.
33	SDATA	Input/Output	Pullup	I^2C Data Input. Input: LVCMOS/LVTTL interface levels. Output: Open Drain.
35	V_{CCA}	Power		Analog supply pin.
36	LOCK	Output		PLL Lock Indicator. LVCMOS/LVTTL interface levels.
39	CLK_SEL	Input	Pulldown	Input source control pin. LVCMOS/LVTTL interface levels. 0 = XTAL (default) 1 = CLK, nCLK

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			3.5		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Frequency Configuration

Table 3A. Frequency Configuration Examples

Output Frequencies (MHz)	Input Frequency or Crystal Frequency (MHz)	Input Clock Divider P	Input Clock Prescaler PS	Feedback Divider M	Output Divider N	VCO Frequency (MHz)
30.72	30.72	1	x2	32	64	1966.08
61.44	30.72	1	x2	32	32	1966.08
62.5	25	1	x2	40	32	2000
76.8	30.72	1	x2	40	32	2457.6
78.125	25	1	x2	50	32	2500
100	25	1	x2	40	20	2000
106.25	26.5625	1	x2	40	20	2125
122.8	30.72	1	x2	32	16	1966.08
125	25	1	x2	40	16	2000
133.33	25	1	x2	48	18	2400
148.5	27	1	x2	44	16	2376
150	25	1	x2	42	14	2100
153.6	30.72	1	x2	40	16	2457.6
155.52	19.44	1	x2	64	16	2488.32
156.25	25	1	x2	50	16	2500
	100	2	x1	50	16	2500
	125	5	x2	50	16	2500
159.375	26.5625	1	x2	36	12	1912.5
160	20	1	x2	48	12	1920
166.66	25	1	x2	40	12	2000
184.32	30.72	1	x2	36	12	2211.84
	61.44	1	x1	36	12	2211.84
187.5	25	1	x1	90	12	2250
200	25	1	x2	40	10	2000
212.5	26.5625	1	x2	40	10	2125
250	25	1	x2	40	8	2000
300	25	1	x2	48	8	2400
311.04	19.44	1	x2	64	8	2488.32
	77.76	1	x1	32	8	2488.32
	155.52	2	x1	32	8	2488.32
312.5	25	1	x2	50	8	2500
	125	2	x1	40	8	2500
	156.25	5	x2	40	8	2500
318.75	26.5625	1	x2	36	6	1912.5
322.265625	25.78125	2	x1	150	6	1933.59375
375	25	1	x1	90	6	2250
400	25	1	x2	40	5	2000
425	26.5625	1	x2	40	5	2125
491.52	30.72	1	x2	32	4	1966.08
614.4	30.72	1	x2	40	4	2457.6
	122.88	2	x1	40	4	2457.6
	153.6	5	x2	40	4	2457.6
622.08	19.44	1	x2	64	4	2488.32
625	25	1	x2	50	4	2500
1228.88	30.72	1	x2	40	2	2457.6

NOTE: Each device supports 4 output frequencies (with related input or crystal value) as selected from this table Register Settings.
NOTE: XTAL operation: $f_{OUT} = f_{REF} * PS * M / N$; CLK, nCLK input operation: $f_{OUT} = (f_{REF} / P) * PS * M / N$.

Table 3B. I^2C Register Map

Register	Binary Register Address	Register Bit							
		D7	D6	D5	D4	D3	D2	D1	D0
0	00000	M0[8]	M0[7]	M0[6]	M0[5]	M0[4]	M0[3]	M0[2]	M0[1]
1	00001	M1[8]	M1[7]	M1[6]	M1[5]	M1[4]	M1[3]	M1[2]	M1[1]
2	00010	M2[8]	M2[7]	M2[6]	M2[5]	M2[4]	M2[3]	M2[2]	M2[1]
3	00011	M3[8]	M3[7]	M3[6]	M3[5]	M3[4]	M3[3]	M3[2]	M3[1]
4	00100	unused	N0[6]	N0[5]	N0[4]	N0[3]	N0[2]	N0[1]	N0[0]
5	00101	unused	N1[6]	N1[5]	N1[4]	N1[3]	N1[2]	N1[1]	N1[0]
6	00110	unused	N2[6]	N2[5]	N2[4]	N2[3]	N2[2]	N2[1]	N2[0]
7	00111	unused	N3[6]	N3[5]	N3[4]	N3[3]	N3[2]	N3[1]	N3[0]
8	01000	unused	BYPASS0	PS0[1]	PS0[0]	P0[1]	P0[0]	CP0[1]	CP0[0]
9	01001	unused	BYPASS1	PS1[1]	PS1[0]	P1[1]	P1[0]	CP1[1]	CP1[0]
10	01010	unused	BYPASS2	PS2[1]	PS2[0]	P2[1]	P2[0]	CP2[1]	CP2[0]
11	01011	unused	BYPASS3	PS3[1]	PS3[0]	P3[1]	P3[0]	CP3[1]	CP3[0]
12	01100	LVDS_ SEL0[Q7]	LVDS_ SEL0[Q6]	LVDS_ SEL0[Q5]	LVDS_ SEL0[Q4]	LVDS_ SEL0[Q3]	LVDS_ SEL0[Q2]	LVDS_ SEL0[Q1]	LVDS_ SEL0[Q0]
13	01101	LVDS_ SEL1[Q7]	LVDS_ SEL1[Q6]	LVDS_ SEL1[Q5]	LVDS_ SEL1[Q4]	LVDS_ SEL1[Q3]	LVDS_ SEL1[Q2]	LVDS_ SEL1[Q1]	LVDS_ SEL1[Q0]
14	01110	LVDS_ SEL2[Q7]	LVDS_ SEL2[Q6]	LVDS_ SEL2[Q5]	LVDS_ SEL2[Q4]	LVDS_ SEL2[Q3]	LVDS_ SEL2[Q2]	LVDS_ SEL2[Q1]	LVDS_ SEL2[Q0]
15	01111	LVDS_ SEL3[Q7]	LVDS_ SEL3[Q6]	LVDS_ SEL3[Q5]	LVDS_ SEL3[Q4]	LVDS_ SEL3[Q3]	LVDS_ SEL3[Q2]	LVDS_ SEL3[Q1]	LVDS_ SEL3[Q0]
16	10000	OE0[Q7]	OE0[Q6]	OE0[Q5]	OE0[Q4]	OE0[Q3]	OE0[Q2]	OE0[Q1]	OE0[Q0]
17	10001	OE1[Q7]	OE1[Q6]	OE1[Q5]	OE1[Q4]	OE1[Q3]	OE1[Q2]	OE1[Q1]	OE1[Q0]
18	10010	OE2[Q7]	OE2[Q6]	OE2[Q5]	OE2[Q4]	OE2[Q3]	OE2[Q2]	OE2[Q1]	OE2[Q0]
19	10011	OE3[Q7]	OE3[Q6]	OE3[Q5]	OE3[Q4]	OE3[Q3]	OE3[Q2]	OE3[Q1]	OE3[Q0]
20	10100	reserved	reserved	reserved	reserved	reserved	reserved	unused	unused
21	10101	unused	unused	unused	unused	unused	unused	unused	unused
22	10110	unused	unused	unused	unused	unused	unused	unused	unused
23	10111	unused	unused	unused	unused	unused	unused	unused	unused

Table 3C. I^2C Function Descriptions

Bits	Name	Function
Pn[1:0]	Input Clock Divider Register n (n = 0...3)	Sets the PLL input clock divider. The divider value has the range of 1, 2, 4 and 5. See Table 3F. Pn[1:0] bits are programmed with values to support default configuration settings for FSEL[1:0].
PSn(1:0)	Input Prescaler Register n (n = 0...3)	Sets the PLL input clock prescaler value. Valid prescaler values are x0.5, x1 or x2. See Table 3F. Set prescaler to x2 for optimum phase noise performance. PSn[1:0] bits are programmed with values to support default configuration settings for FSEL[1:0].
Mn[8:1]	Integer Feedback Divider Register n (n = 0...3)	Sets the integer feedback divider value. Based on the FemtoClock NG VCO range, the applicable feedback dividers settings are 16 thru 250. Please note the register value presents bits [8:1] of Mn, the LSB of Mn is not in the register. Mn[8:1] bits are programmed with values to support default configuration settings for FSEL[1:0].
Nn[6:0]	Output Divider Register n (n = 0...3)	Sets the output divider. The output divider value can range from 2, 3, 4, 5, 6 and 8, 10, 12 to 126 (step: 2). See Table 3G for the output divider coding. Nn[6:0] bits are programmed with values to support default configuration settings for FSEL[1:0].
CPn[1:0]	PLL Bandwidth Register n (n = 0...3)	Sets the FemtoClock NG PLL bandwidth by controlling the charge pump current. See Table 3H. CPn[1:0] bits are programmed with values to support default configuration settings for FSEL[1:0].
BYPASSn	PLL Bypass Register n (n = 0...3)	Bypasses PLL. Output of the prescaler is routed through the output divider N to the output fanout buffer. Programming a 1 to this bit bypasses the PLL. Programming a 0 to this bit routes the output of the prescaler through the PLL. BYPASSn bits are programmed with values to support default configuration settings for FSEL[1:0].
OEn[Q0] OEn[Q1] OEn[Q2] OEn[Q3] OEn[Q4] OEn[Q5] OEn[Q6] OEn[Q7]	Output Enable Register n (n = 0...3)	Sets the outputs to Active or High Impedance. Programming a 0 to this bit sets the outputs to High Impedance. Programming a 1 sets the outputs to active status. OEn[Q0], OEn[Q1], OEn[Q2], OEn[Q3], OEn[Q4], OEn[Q5], OEn[Q6], OEn[Q7] bits are programmed with values to support default configuration settings for FSEL[1:0].
LVDS_SELn[Q0] LVDS_SELn[Q1] LVDS_SELn[Q2] LVDS_SELn[Q3] LVDS_SELn[Q4] LVDS_SELn[Q5] LVDS_SELn[Q6] LVDS_SELn[Q7]	Output Style Register n (n = 0...3)	Sets the differential output style to either LVDS or LVPECL interface levels. Programming a 1 to this bit sets the output styles to LVDS levels. Programming a 0 to this bit sets the output styles to LVPECL levels. LVDS_SELn[Q0], LVDS_SELn[Q1], LVDS_SELn[Q2], LVDS_SELn[Q3] LVDS_SELn[Q4], LVDS_SELn[Q5], LVDS_SELn[Q6], LVDS_SELn[Q7] bits are programmed with values to support default configuration settings for FSEL[1:0].

Table 3D. Feedback Divider Mn Coding

Register Bit Mn[8:1]	Feedback Divider Mn
Do Not Use	1 thru 15
00001000	16
00001001	18
00001010	20
00001011	22
00001100 thru 00011111	24 thru 62
00100000	64
00100001	66
00100010	68
00100011	70
00100100	72
...	Mn
00110010	100
00110011	102
00110100	104
00110101	106
...	Mn
01111010	244
01111011	246
01111100	248
01111101	250

Note: Mn is always an even value. The Mn[0] bits are not implemented.

Table 3E. PLL Pre-Scaler P Coding

CLK_SEL	Input	P[1:0]	PS[1:0]	Input Clock Divider P	Input Clock Prescaler PS	Input Frequency (MHz)	
						Minimum	Maximum
0	XTAL	xx	00	1	x1	10	40
			01	1	x0.5	20	40
			1x	1	x2	5	40
1	CLK	00	00	1	x1	10	120
			01	1	x0.5	20	240
			1x	1	x2	5	60
		01	00	2	x1	20	240
			01	2	x0.5	40	480
			1x	2	x2	10	120
		10	00	4	x1	40	480
			01	4	x0.5	80	800
			1x	4	x2	20	240
		11	00	5	x1	50	600
			01	5	x0.5	100	800
			1x	5	x2	25	300

Table 3F. PLL Post Divider N Coding

Register Bit	Output Divider	Output Frequency Range	
N_n[6:0]	N	f_{OUT_MIN} (MHz)	f_{OUT_MAX} (MHz)
000000X	2	Do Not Use	
0000010	2	955	1250
0000011	3	636.67	833.33
0000100	4	477.5	625
0000101	5	382	500
000011X	6	318.33	416.67
000100X	8	238.75	312.5
000101X	10	191	250
000110X	12	159.1667	208.33
000111X	14	136.4286	178.57
001000X	16	119.375	156.25
...	N (even integer)	(1910 ÷ *N*)	(2500 ÷ *N*)
111101X	124	15.40	20.16
111111X	126	15.16	19.84

NOTE: X denotes “don’t care”.

Table 3G. FemtoClock NG PLL Bandwidth Coding

Register Bit		Feedback Divider Value Range	
CPn1	CPn0	Minimum	Maximum
0	0	16	48
0	1	48	100
1	0	100	250
1	1	192	250

NOTE: FemtoClock NG PLL stability is only guaranteed over the feedback divider ranges listed is Table 3G.

Power-up Default Configuration Description

The IDT8T49N008I supports a variety of options such as different output styles, number of programmed default frequencies, output enable and operating temperature range. The device options and default frequencies must be specified at the time of order and are programmed by IDT prior to shipment. The document, *Programmable FemtoClock® NG Product Ordering Guide* specifies the available order codes, including the device options and default frequency configurations. Example part number: 8T49N004A-007NLGI, specifies a quad frequency clock generator with default frequencies of 106.25MHz, 133.333MHz, 156.25MHz and 156.25MHz, with four LVDS outputs that are enabled after power-up, specified over the industrial temperature range and housed in a lead-free (6/6 RoHS) VFQFN package.

Other order codes with respective programmed frequencies are available from IDT upon request. After power-up changes to the output frequencies are controlled by FSEL[1:0] or the I^2C interface. Changes to the output styles and states of outputs (enabled or disabled) can also be controlled with the I^2C interface after power up.

Table 3H. Power-up Default Settings

FSEL1	FSEL0	Frequency	PLL State (On or Bypass)	Output State (Active or High Impedance)	Output Style (LVDS or LVPECL)
0 (default)	0 (default)	Frequency 0	PLL State 0	Output State 0	Output Style 0
0	1	Frequency 1	PLL State 1	Output State 1	Output Style 1
1	0	Frequency 2	PLL State 2	Output State 2	Output Style 2
1	1	Frequency 3	PLL State 3	Output State 3	Output Style 3

Serial Interface Configuration Description

The IDT8T49N008I has an I^2C-compatible configuration interface to access any of the internal registers (Table 3B) for frequency and PLL parameter programming. The IDT849N008I acts as a slave device on the I^2C bus and has the address 0b110111x, where x is set by the value on the ADDR_SEL input (see Tables 3I and 3J). The interface accepts byte-oriented block write and block read operations. An address byte (P) specifies the register address (Table 3B) as the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first, see Table 3K, 3L). Read and write block transfers can be stopped after any complete byte transfer. It is recommended to terminate the I^2C read or write transfer after accessing byte #23 by sending a stop command.

For full electrical I^2C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 50kΩ typical.

Table 3I. I^2C Device Slave Address ADDR_SEL = 0 (default)

1	1	0	1	1	1	0	R/W

Table 3J. I^2C Device Slave Address ADDR_SEL = 1

1	1	0	1	1	1	1	R/W

Table 3K. Block Write Operation

Bit	1	2:8	9	10	11:18	19	20:27	28	29-36	37	...	...	...
Description	START	Slave Address	W (0)	ACK	Address Byte P	ACK	Data Byte (P)	ACK	Data Byte (P+1)	ACK	Data Byte ...	ACK	STOP
Length (bits)	1	7	1	1	8	1	8	1	8	1	8	1	1

Table 3L. Block Read Operation

Bit	1	2:8	9	10	11:18	19	20	21:27	28	29	30:37	38	39-46	47	...	...	...
Description	START	Slave Address	W (0)	ACK	Address byte P	ACK	Repeated START	Slave address	R (1)	ACK	Data Byte (P)	ACK	Data Byte (P+1)	ACK	Data Byte ...	ACK	STOP
Length (bits)	1	7	1	1	8	1	1	7	1	1	8	1	8	1	8	1	1

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	3.63V
Inputs, V_I XTAL_IN Other Input	 0V to 2V -0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current Outputs, I_O (SDATA) Outputs, I_O (LVDS) Continuous Current Surge Current	 50mA 100mA 10mA 10mA 15mA
Package Thermal Impedance, θ_{JA}	32.4°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.32	3.3	V_{CC}	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{CCA}	Analog Supply Current				32	mA
I_{EE}	Power Supply Current	LVPECL			225	mA
I_{CC}	Power Supply Current	LVDS			125	mA
I_{CCO}	Output Supply Current	LVDS			162	mA

Table 4B. Power Supply DC Characteristics, $V_{CC} = V_{CCO} = 2.5V \pm 5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.28	2.5	V_{CC}	V
V_{CCO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{CCA}	Analog Supply Current				28	mA
I_{EE}	Power Supply Current	LVPECL			216	mA
I_{CC}	Power Supply Current	LVDS			122	mA
I_{CCO}	Output Supply Current	LVDS			160	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	SCLK, SDATA, FSEL[1:0], CLK_SEL, ADDR_SEL	$V_{CC} = 3.3V$	2		$V_{CC} + 0.3$	V
			$V_{CC} = 2.5V$	1.7		$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	SCLK, SDATA, CLK_SEL, ADDR_SEL	$V_{CC} = 3.3V$	-0.3		0.8	V
			$V_{CC} = 2.5V$	-0.3		0.7	V
		FSEL[1:0],	$V_{CC} = 3.3V$ or $2.5V$			0.5	V
I_{IH}	Input High Current	SCLK, SDATA	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$			5	µA
		FSEL[1:0], CLK_SEL, ADDR_SEL	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$			150	µA
I_{IL}	Input Low Current	SCLK, SDATA	$V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-150			µA
		FSEL[1:0], CLK_SEL, ADDR_SEL	$V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-5			µA
V_{OH}	Output High Voltage; NOTE 1	LOCK	$V_{CC} = 3.465V$	2.6			V
		LOCK	$V_{CC} = 2.625V$	1.8			V
V_{OL}	Output Low Voltage; NOTE 1	LOCK	$V_{CC} = 3.465V$ or $2.625V$			0.5	V

NOTE 1: Output terminated with 50Ω to $V_{CCO}/2$. See Parameter Measurement Information, *Output Load Test Circuit* diagrams.

Table 4D. Differential DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$			150	µA
I_{IL}	Input Low Current	nCLK	$V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-150			µA
		CLK	$V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-5			µA
V_{PP}	Peak-to-Peak Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1			V_{EE}		$V_{CC} - 0.85$	V

NOTE 1: Common mode input voltage is at the cross point.

Table 4E. LVPECL DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CC} - 1.1$		$V_{CCO} - 0.75$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CCO} - 1.6$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with 50Ω to $V_{CC} - 2V$.

Table 4F. LVPECL DC Characteristics, $V_{CC} = V_{CCO} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CC} – 1.2$		$V_{CCO} – 0.75$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CC} – 2.0$		$V_{CC} – 1.5$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.5		1.0	V

NOTE 1: Outputs termination with 50Ω to $V_{CC} – 2V$.

Table 4G. LVDS DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247	345	454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.15	1.25	1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 4H. LVDS DC Characteristics, $V_{CC} = V_{CCO} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		230	340	454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.15	1.25	1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		10		40	MHz
Load Capacitance (C_L)		10		18	pF
Equivalent Series Resistance (ESR)				50	Ω

AC Electrical Characteristics

Table 6A. PCI Express Jitter Specifications, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	PCIe Industry Specification	Units
t_j (PCIe Gen 1)	Phase Jitter Peak-to-Peak; NOTE 1, 4	f = 100MHz, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2)		8.3	13.2	86	ps
$t_{REFCLK\_HF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	f = 100MHz, 25MHz Crystal Input High Band: 1.5MHz - Nyquist (clock frequency/2)		0.78	1.35	3.1	ps
$t_{REFCLK\_LF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	f = 100MHz, 25MHz Crystal Input Low Band: 10kHz - 1.5MHz		0.05	0.10	3.0	ps
t_{REFCLK_RMS} (PCIe Gen 3)	Phase Jitter RMS; NOTE 3, 4	f = 100MHz, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2)		0.175	0.34	0.8	ps

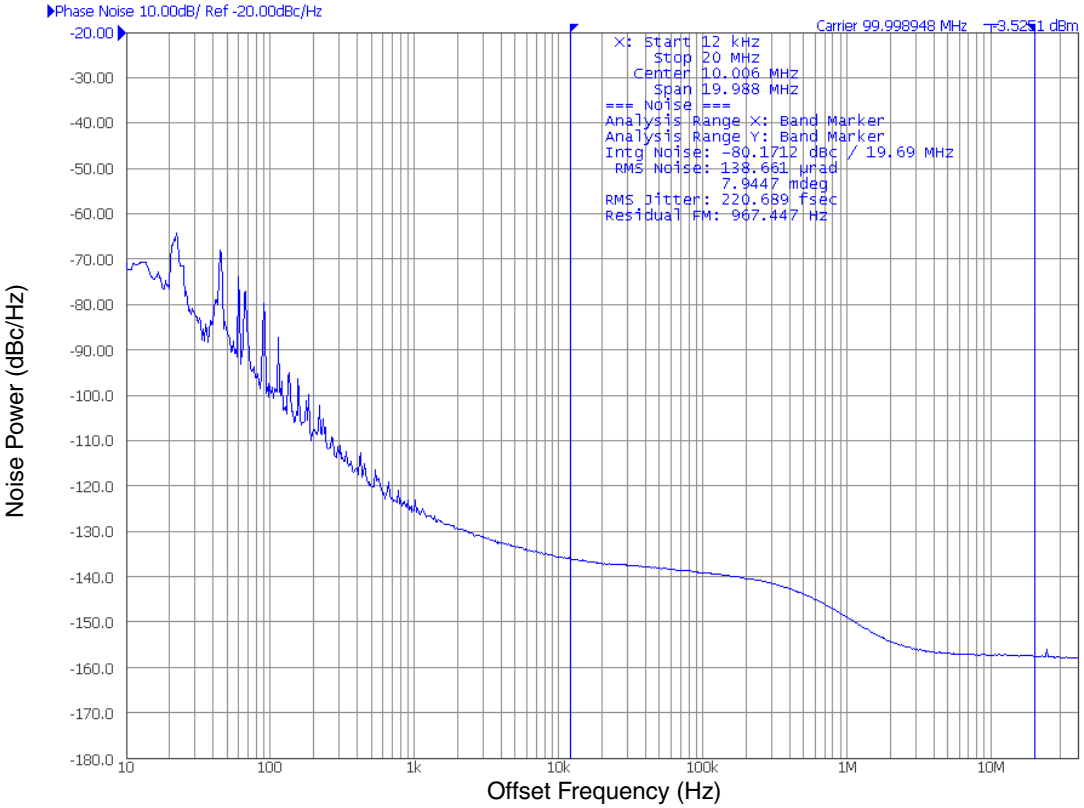
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions. For additional information, refer to the *PCI Express Application Note section* in the datasheet.
NOTE 1: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of 10^6 clock periods.
NOTE 2: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band).
NOTE 3: RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the *PCI Express Base Specification Revision 0.7, October 2009* and is subject to change pending the final release version of the specification.
NOTE 4: This parameter is guaranteed by characterization. Not tested in production.

Table 6B. AC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$ $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

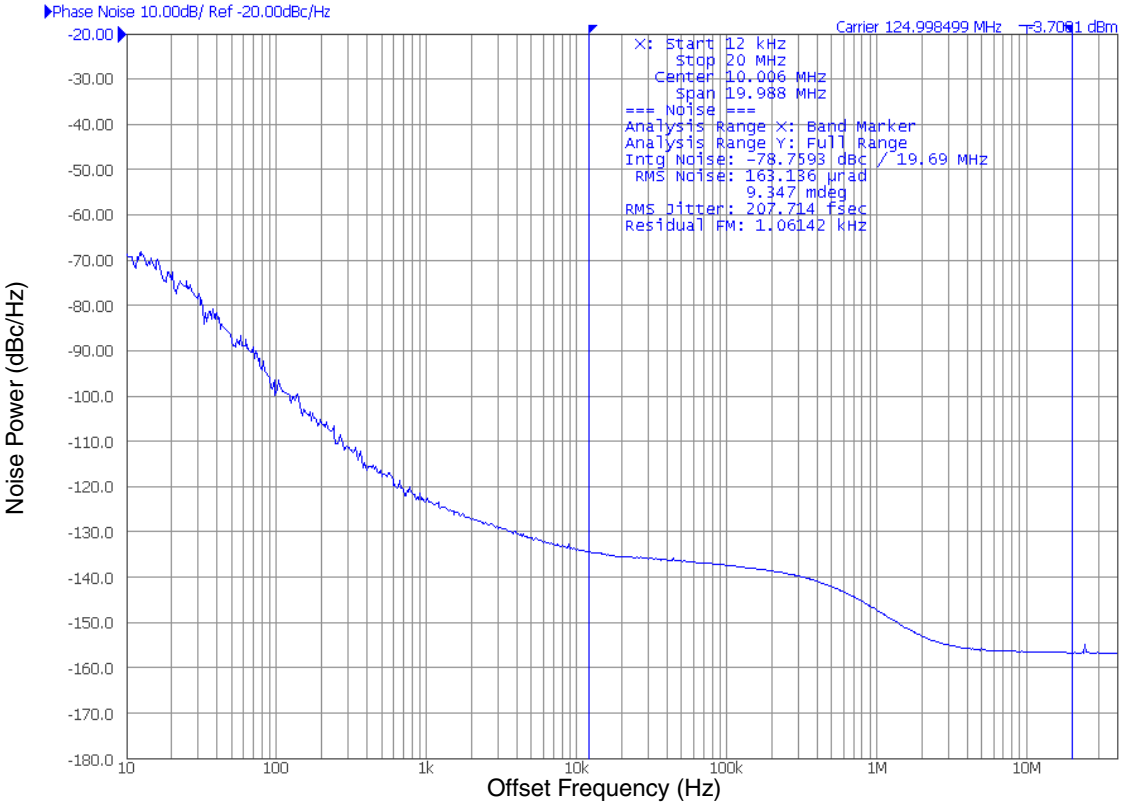
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{DIFF_IN}	Differential Input Frequency			10		312.5	MHz
f_{VCO}	VCO Frequency			1910		2500	MHz
$t_{jit(Ø)}$ RMS Phase Jitter, Random; NOTE 1			25MHz Crystal, f_{OUT} = 100MHz, Integration Range: 12kHz – 20MHz		258	332	fs
			25MHz Crystal, f_{OUT} = 125MHz, Integration Range: 12kHz – 20MHz		220	291	fs
			25MHz Crystal, f_{OUT} = 125MHz, Integration Range: 10kHz – 1MHz		164	232	fs
			25MHz Crystal, f_{OUT} = 156.25MHz, Integration Range: 12kHz – 20MHz		228	306	fs
			25MHz Crystal, f_{OUT} = 156.25MHz, Integration Range: 10kHz – 1MHz		175	234	fs
			25MHz Crystal, f_{OUT} = 250MHz, Integration Range: 12kHz – 20MHz		212	292	fs
			30.72MHz Crystal, f_{OUT} = 491.52MHz, Integration Range: 12kHz – 20MHz		213	299	fs
			19.44MHz Crystal, f_{OUT} = 622.08MHz, Integration Range: 12kHz – 20MHz		280	386	fs
tsk(o)	Output Skew; NOTE 2, 3	LVPECL Outputs	LVDS_SEL = 0			50	ps
		LVDS Outputs	LVDS_SEL = 1			50	ps
t_R / t_F	Output Rise/Fall Time	LVPECL Outputs	20% - 80%, LVDS_SEL = 0	100		400	ps
		LVDS Outputs	20% - 80%, LVDS_SEL = 1	100		400	ps
odc	Output Duty Cycle		N > 3 Output Divider; LVDS_SEL = 0 or 1	47		53	%
			N ≤ 3 Output Divider; LVDS_SEL = 0 or 1	42		58	%
t_{LOCK}	PLL Lock Time; NOTE 3, 4	LOCK Output				20	ms
$t_{TRANSITION}$	Transition Time; NOTE 3, 4	LOCK Output				20	ms

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Refer to Phase Noise Plots.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
NOTE 3: These parameters are guaranteed by characterization. Not tested in production.
NOTE 4: Refer to t_{LOCK} and $t_{TRANSITION}$ in Parameter Measurement Information.

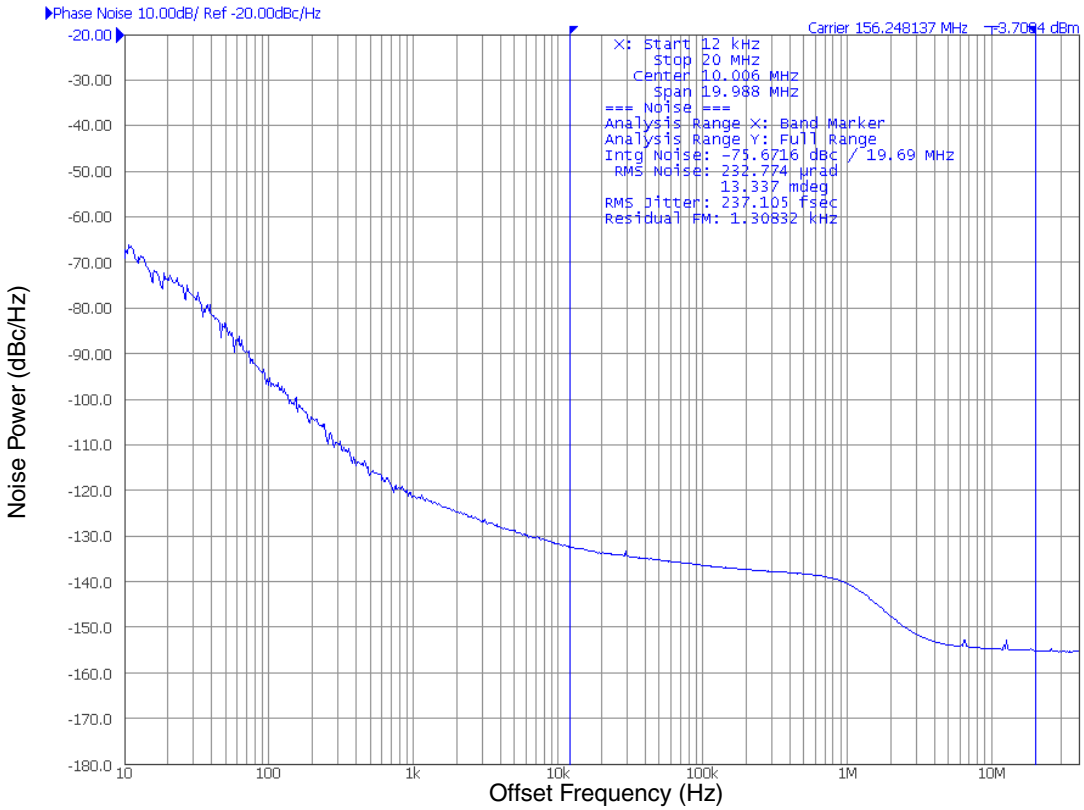
Typical Phase Noise at 100MHz (3.3V)



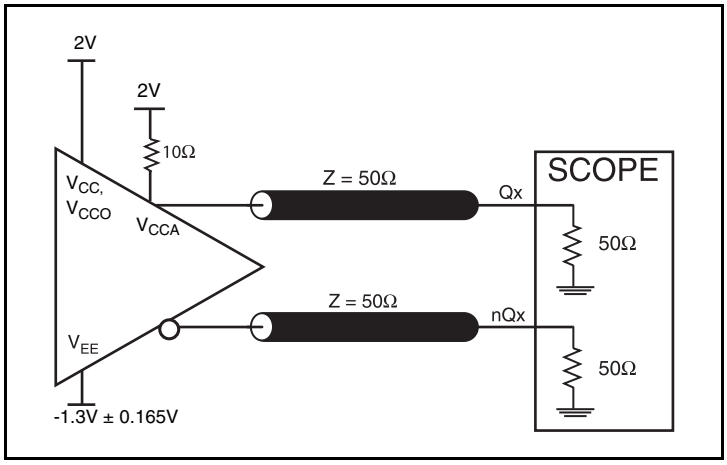
Typical Phase Noise at 125MHz (3.3V)



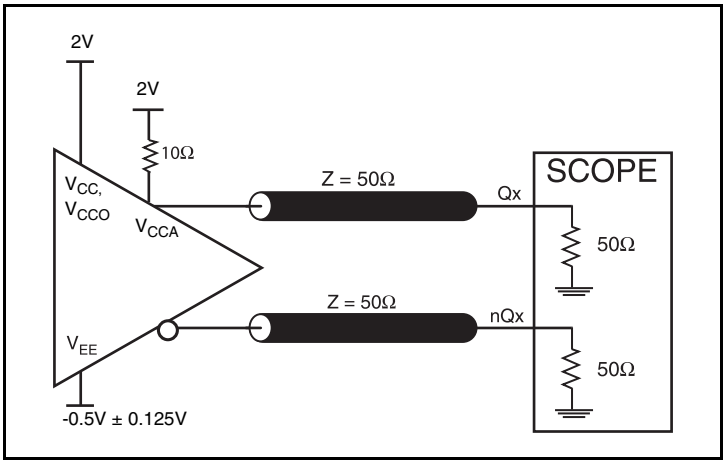
Typical Phase Noise at 156.25MHz (3.3V)



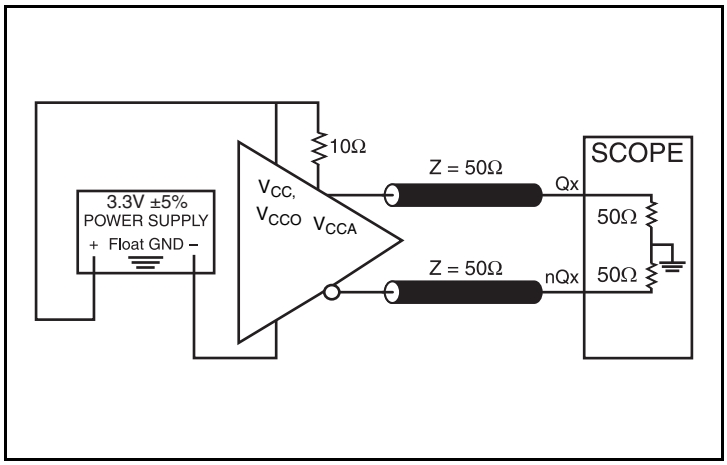
Parameter Measurement Information



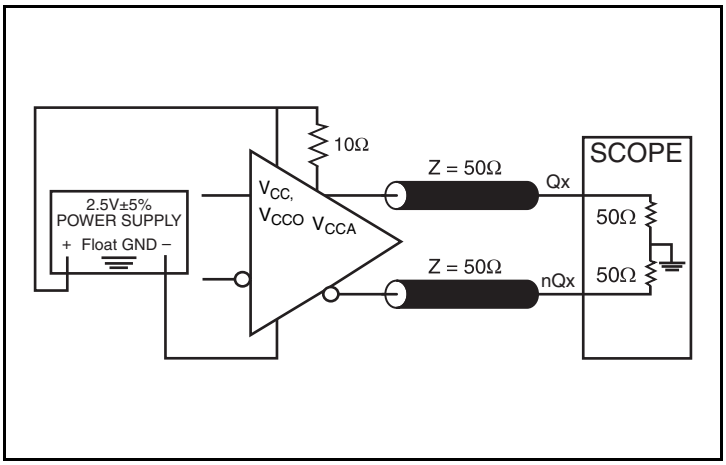
3.3V LVPECL Output Load AC Test Circuit



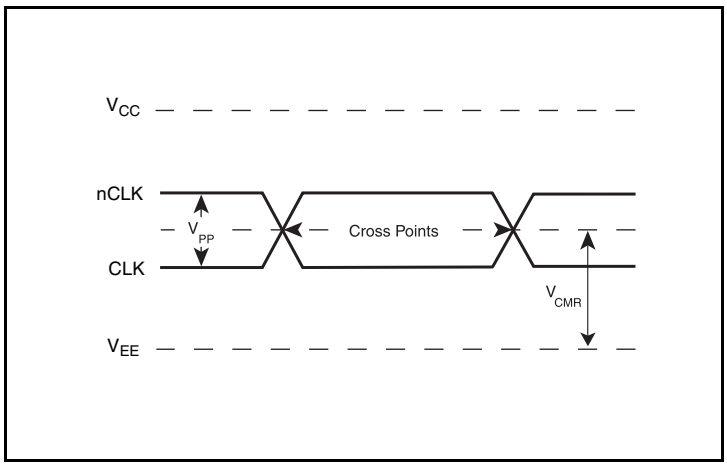
2.5V LVPECL Output Load AC Test Circuit



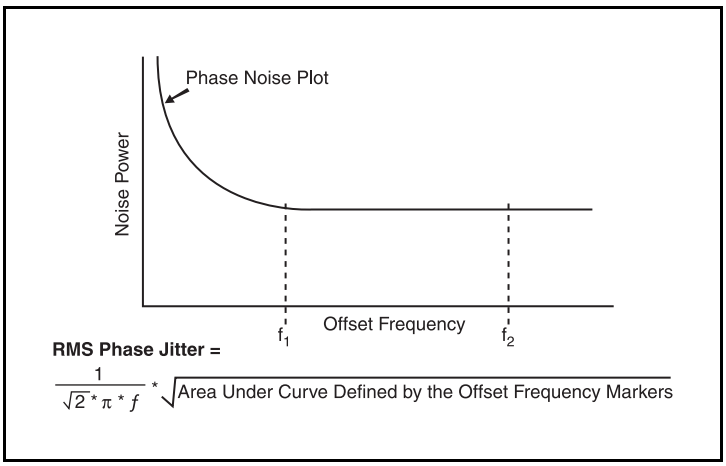
3.3V LVDS Output Load AC Test Circuit



2.5V LVDS Output Load AC Test Circuit

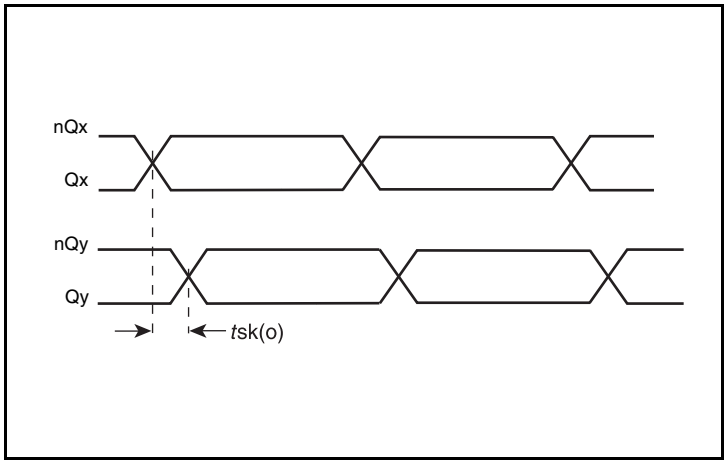


Differential Input Levels

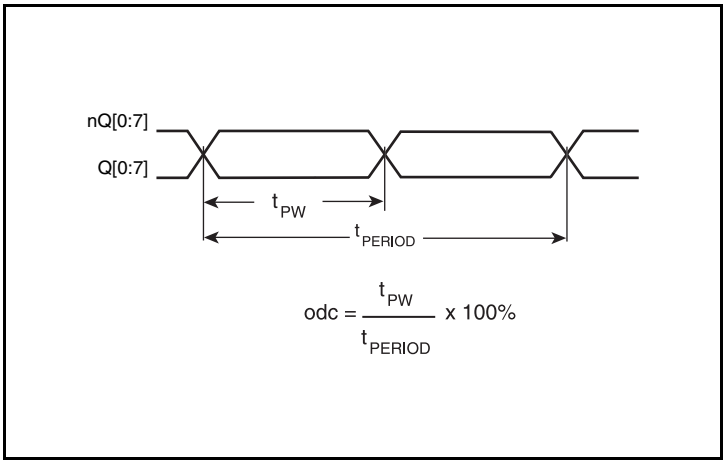


RMS Phase Jitter

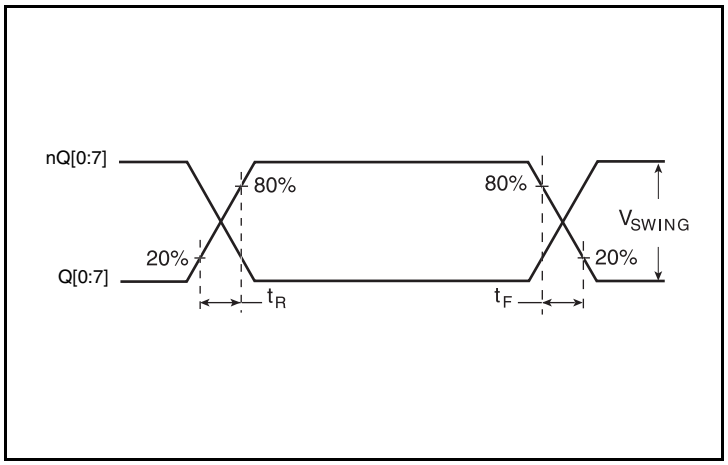
Parameter Measurement Information, continued



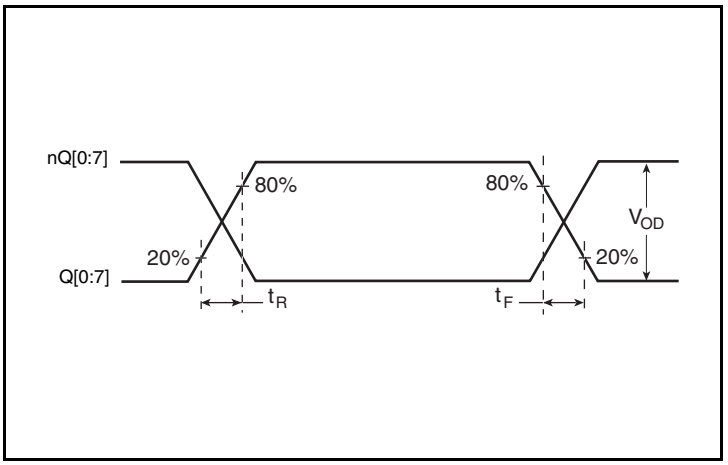
Output Skew



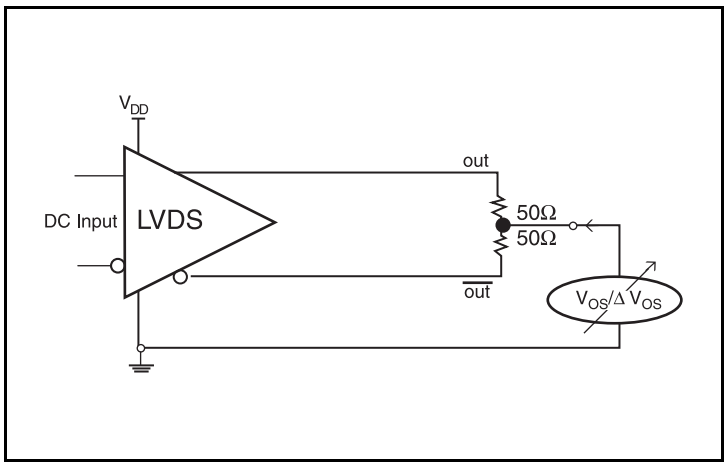
Output Duty Cycle/Pulse Width/Period



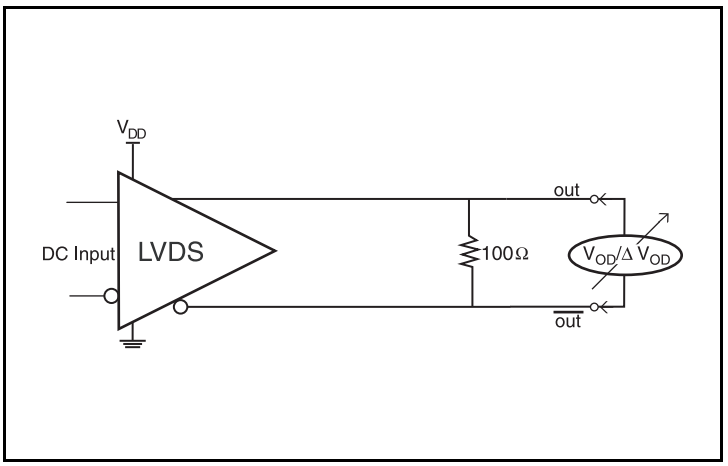
LVPECL Output Rise/Fall Time



LVDS Output Rise/Fall Time

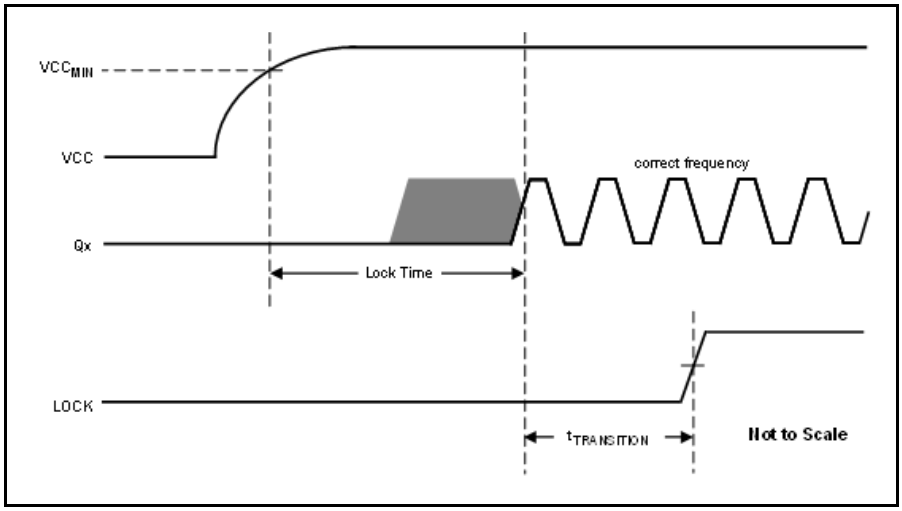


Offset Voltage Setup



Differential Output Voltage Setup

Parameter Measurement Information, continued



Lock Time & Transition Time

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

Outputs:

LVPECL Outputs

All unused LVPECL output pairs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

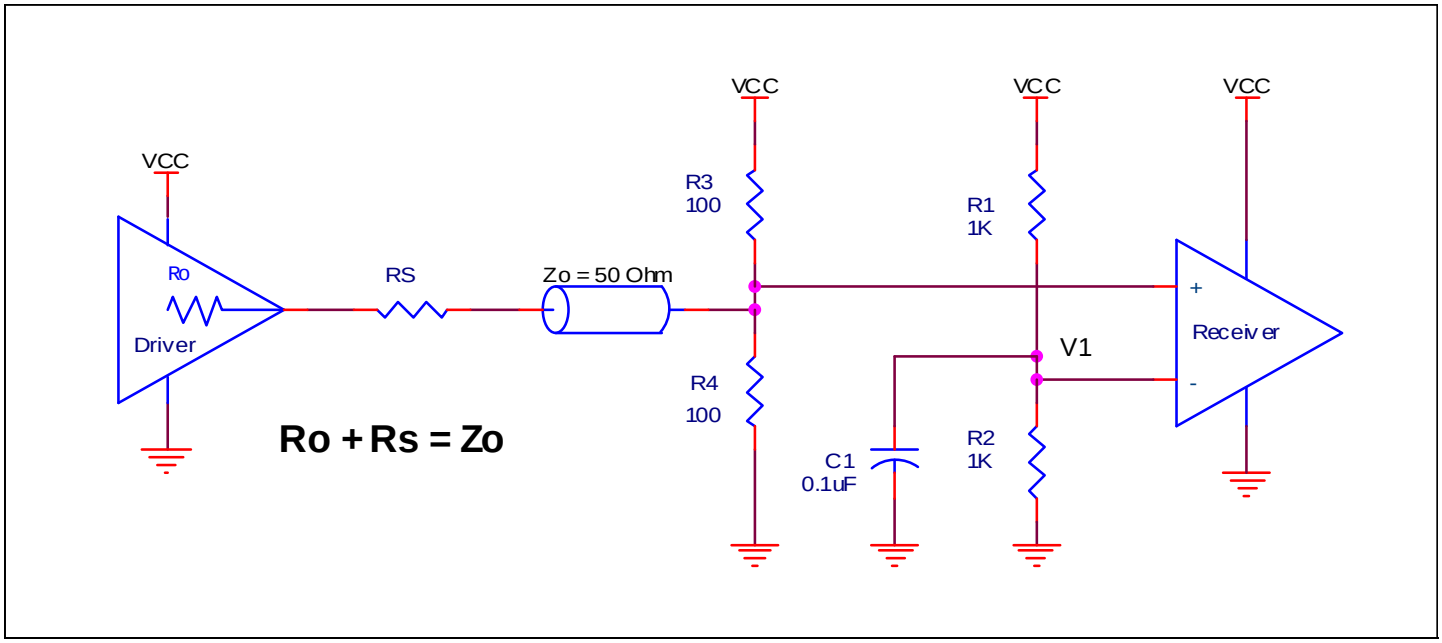


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 2A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 2B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

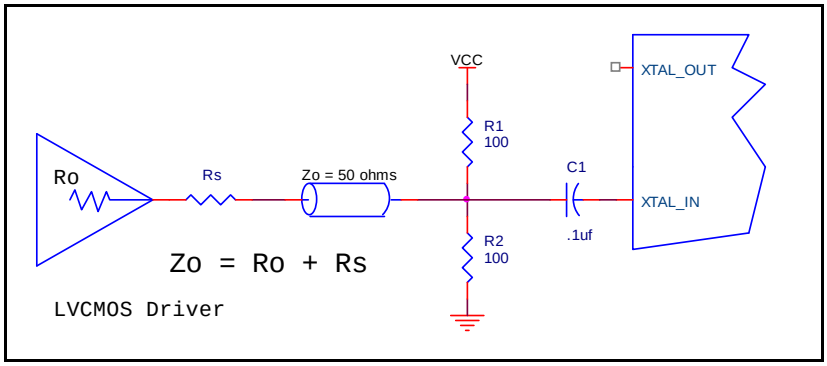


Figure 2A. General Diagram for LVCMOS Driver to XTAL Input Interface

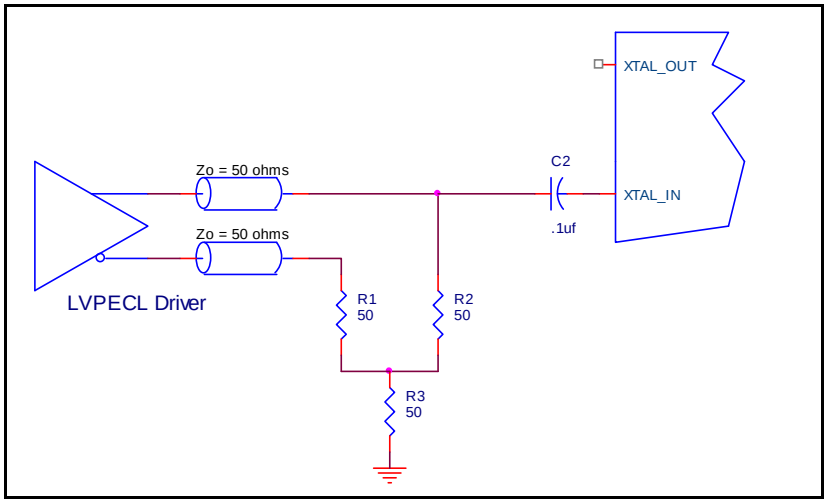


Figure 2B. General Diagram for LVPECL Driver to XTAL Input Interface

3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3D* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

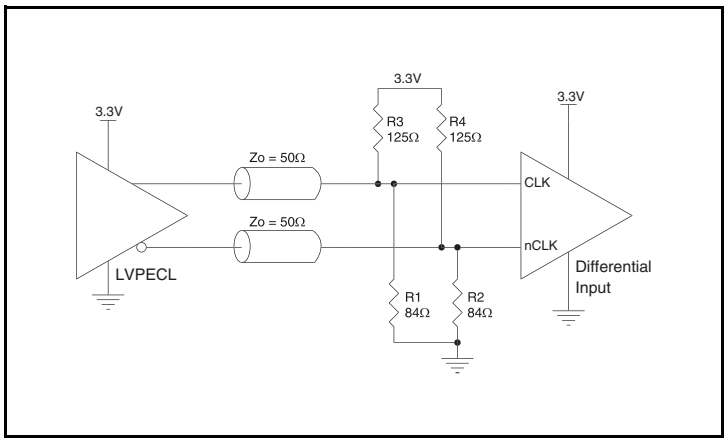


Figure 3A. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

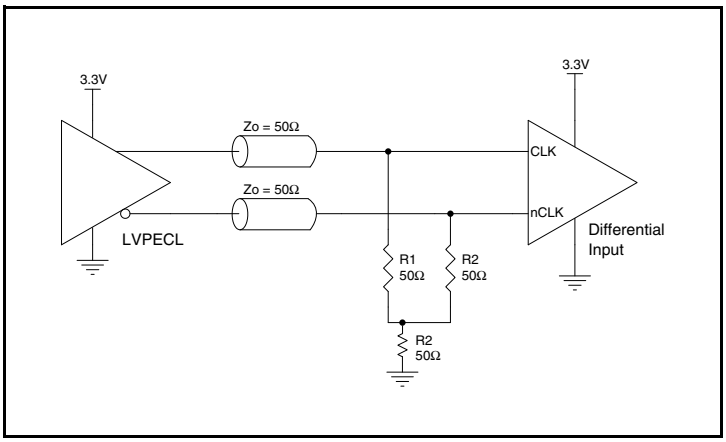


Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

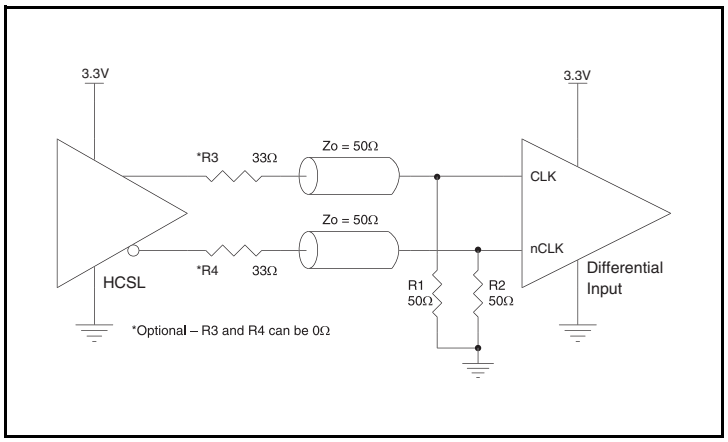


Figure 3C. CLK/nCLK Input Driven by a 3.3V HCSL Driver

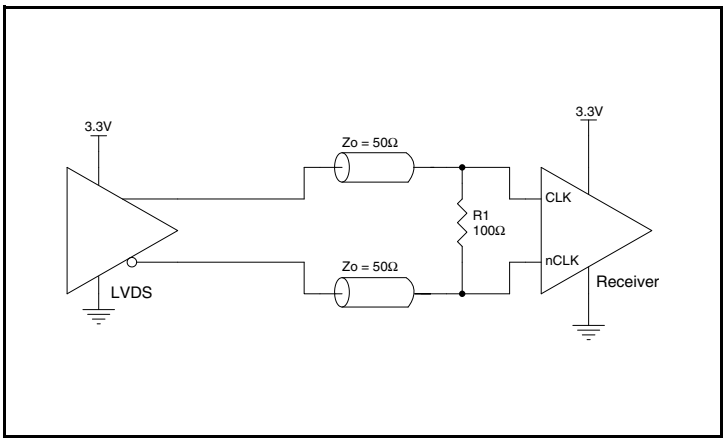


Figure 3D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

2.5V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4D* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

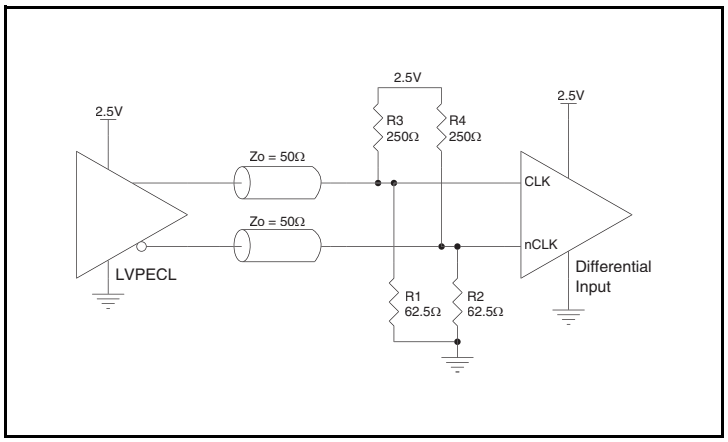


Figure 4A. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

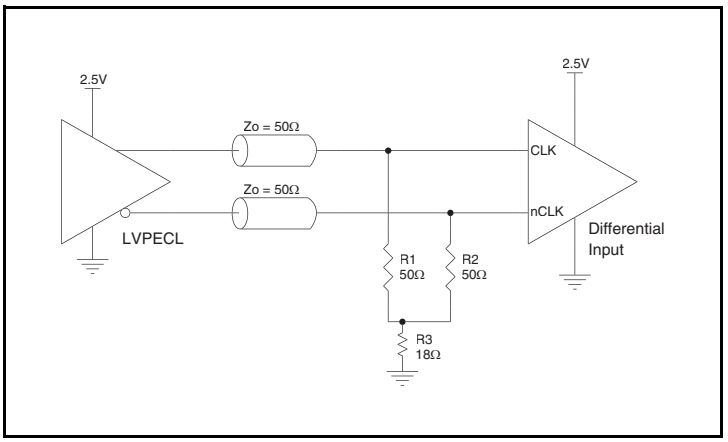


Figure 4B. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

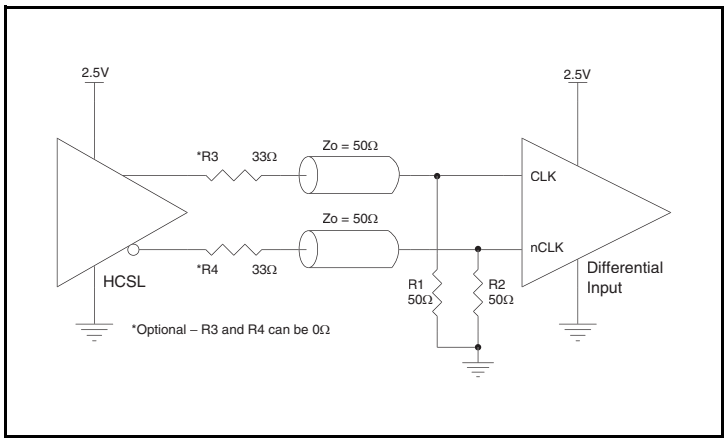


Figure 4C. CLK/nCLK Input Driven by a 2.5V HCSL Driver

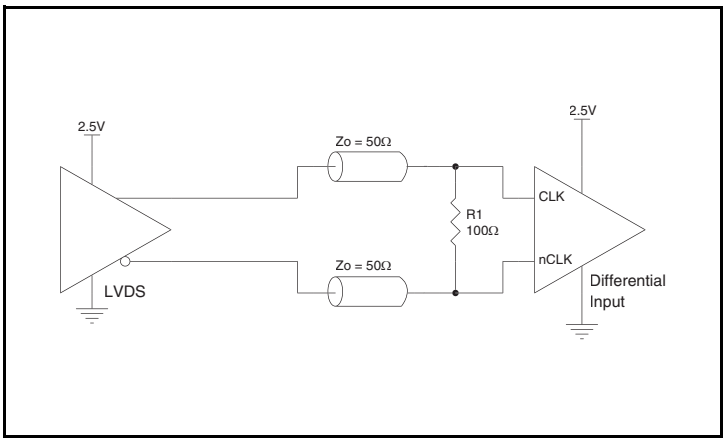


Figure 4D. CLK/nCLK Input Driven by a 2.5V LVDS Driver

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 5A* can be used with either type of output structure. *Figure 5B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

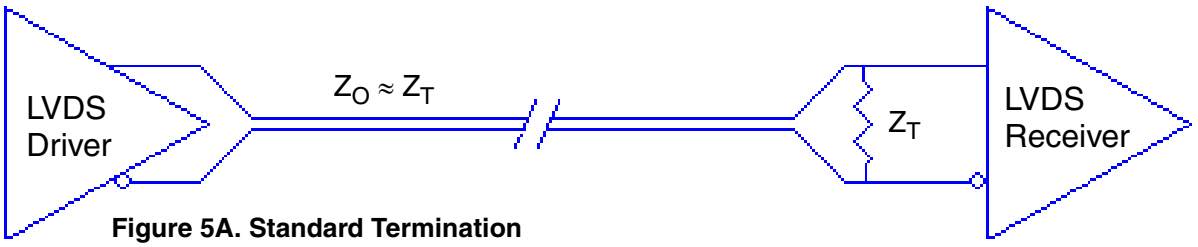


Figure 5A. Standard Termination

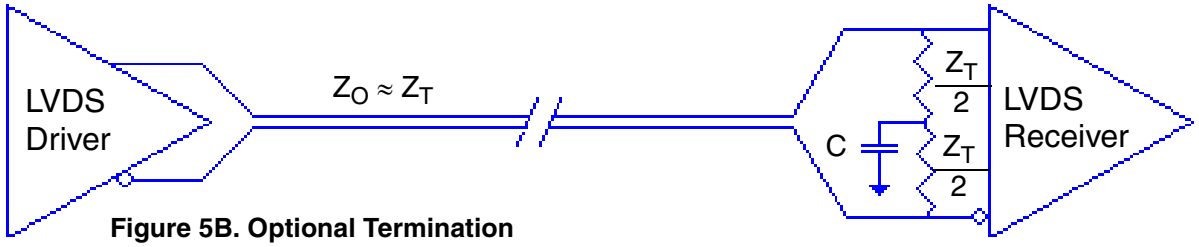


Figure 5B. Optional Termination

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 6A and 6B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

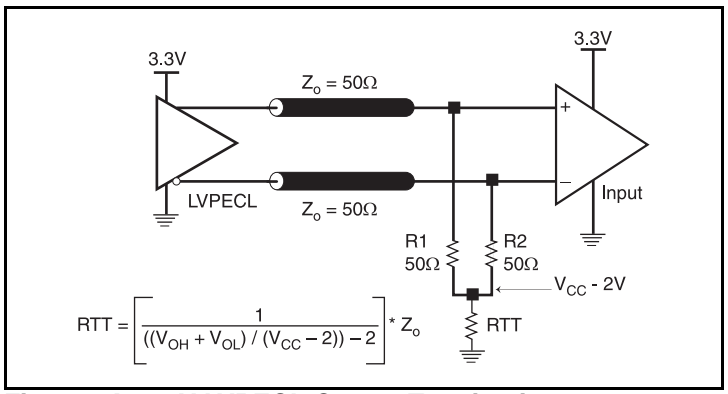


Figure 6A. 3.3V LVPECL Output Termination

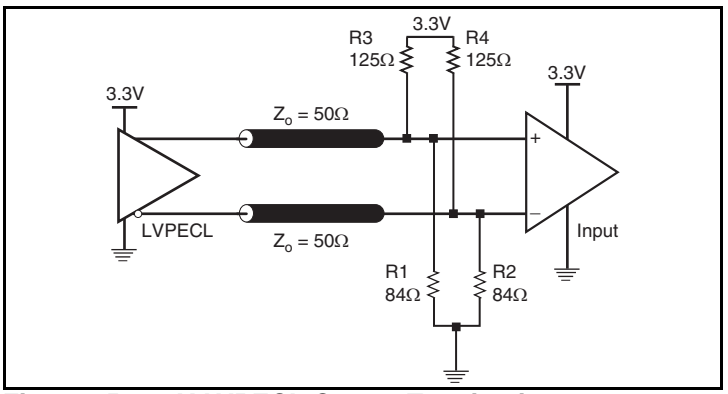


Figure 6B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 7A and *Figure 7B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CCO} – 2V. For V_{CCO} = 2.5V, the V_{CCO} – 2V is very close to ground level. The R3 in Figure 7B can be eliminated and the termination is shown in *Figure 7C.*

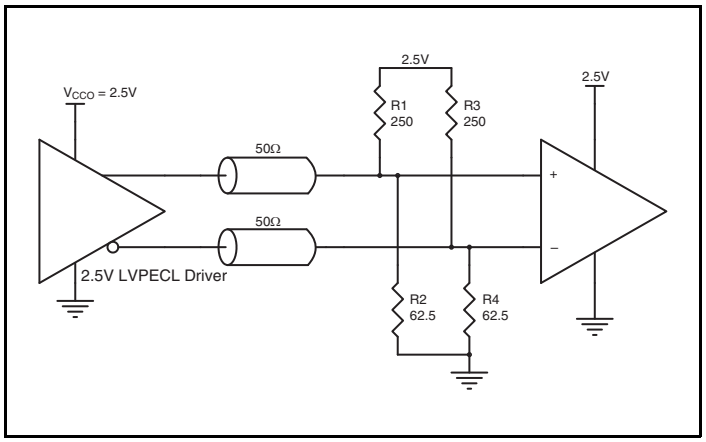


Figure 7A. 2.5V LVPECL Driver Termination Example

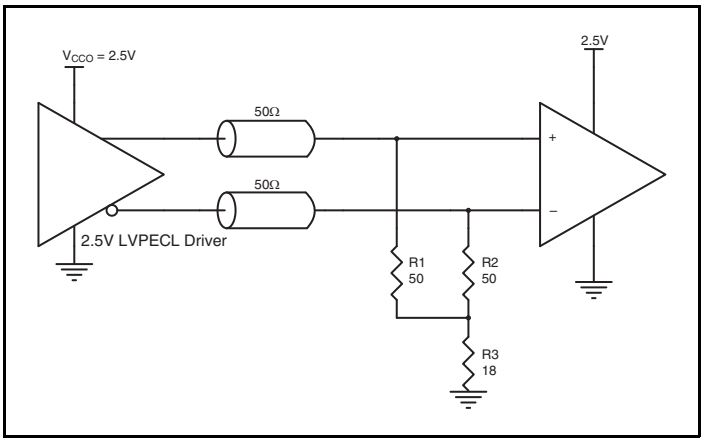


Figure 7B. 2.5V LVPECL Driver Termination Example

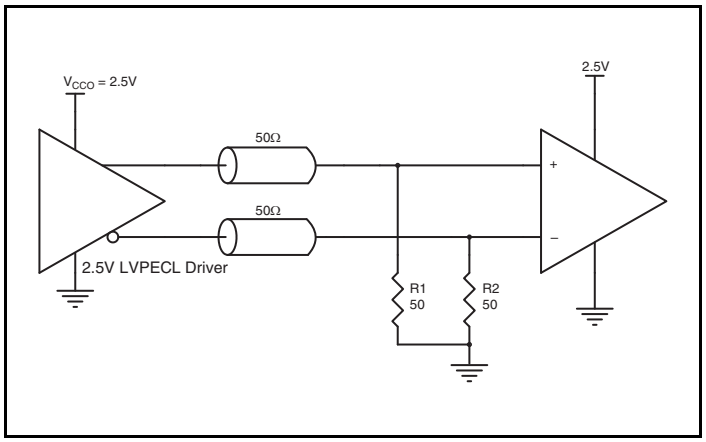


Figure 7C. 2.5V LVPECL Driver Termination Example

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 8.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

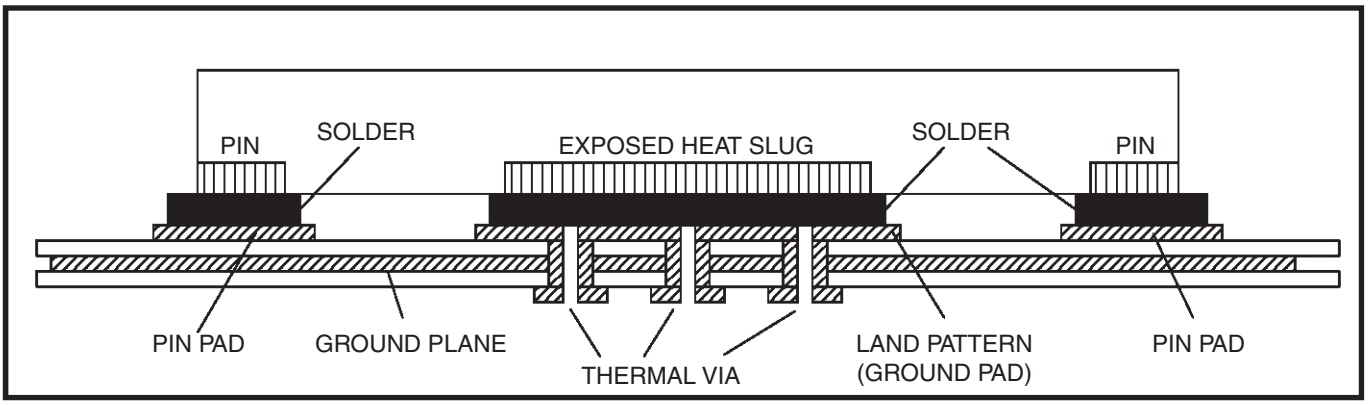


Figure 8. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Schematic Layout

Figure 9 (next page) shows an example of IDT8T49N008I application schematic. The schematic focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

In this example the device is operated at $V_{CC} = V_{CCO} = V_{CCA} = 3.3V$ rather than 2.5V. The CLK, nCLK inputs are provided by a 3.3V LVPECL driver and depicted with a Y-termination rather than the standard four resistor V_{CC} - 2V Thevinin termination for reasons of minimum termination power and layout simplicity. Three examples of PECL terminations are shown for the outputs to demonstrate mixing of PECL termination design options.

As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power supply isolation is required. The IDT8T49N006I provides separate power supplies to isolate from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side. Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices.

The V_{CC} and V_{CCO} filters start to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

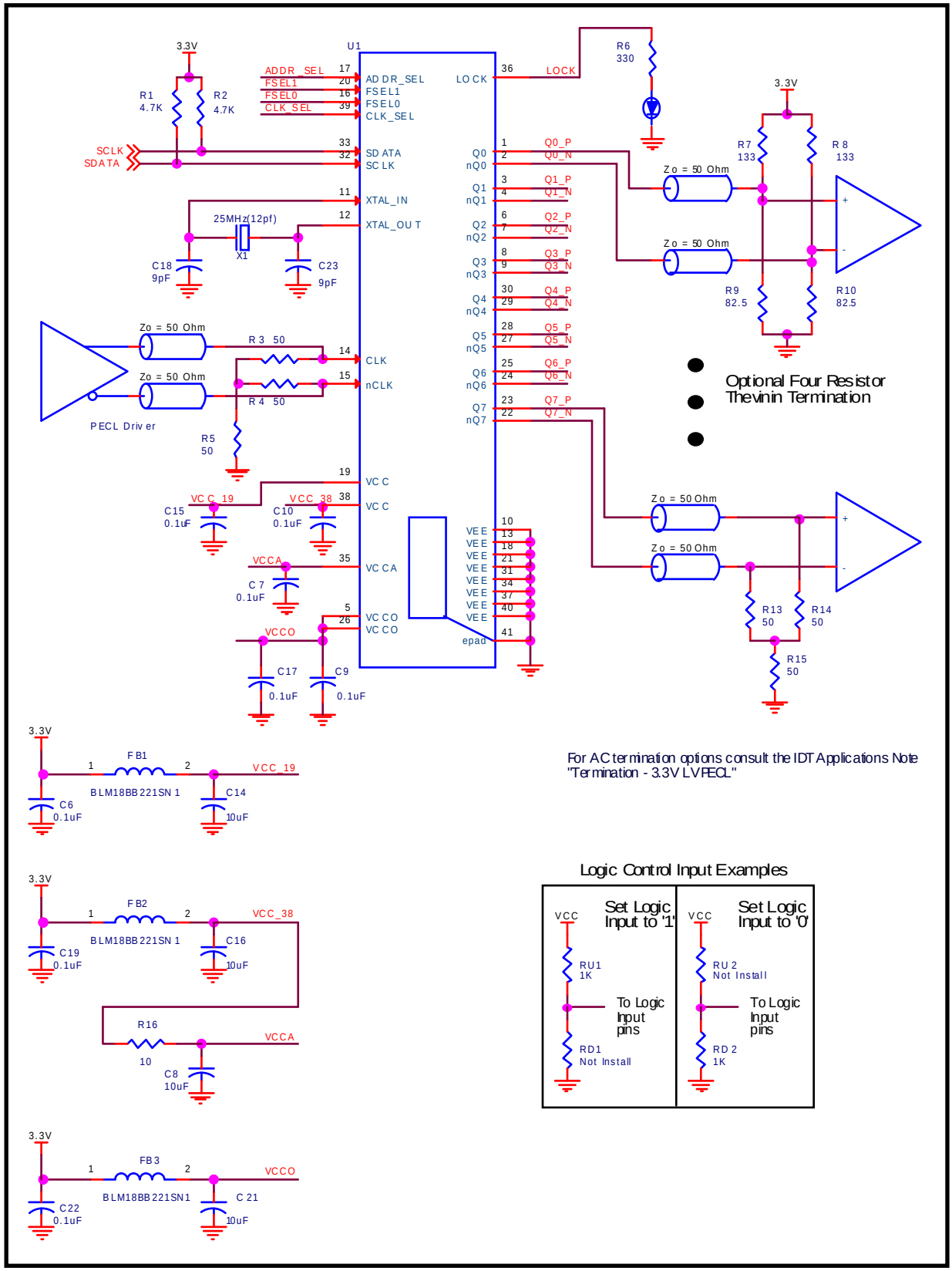


Figure 9. IDT8T49N008I Application Schematic

PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

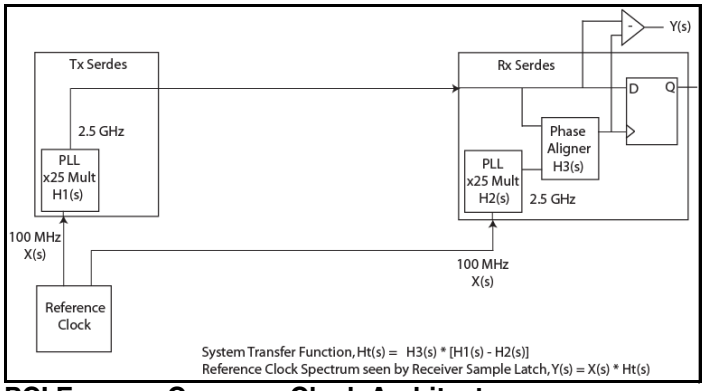
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

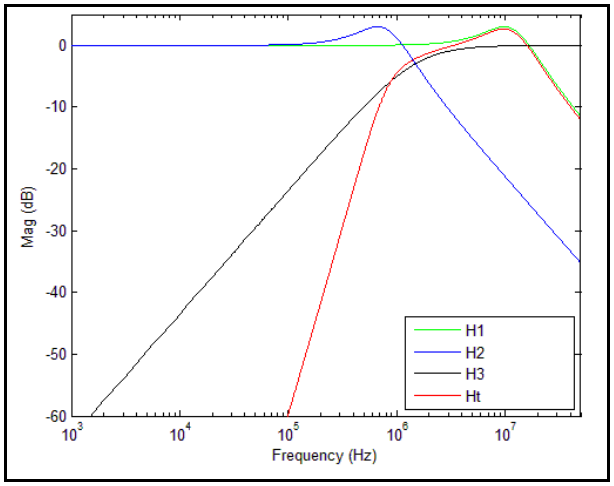
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].



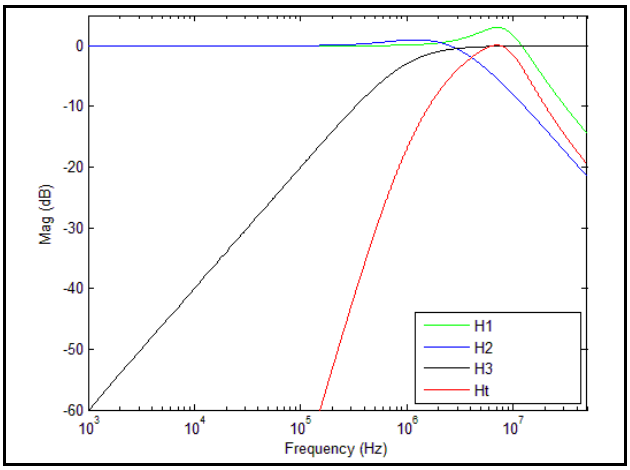
PCI Express Common Clock Architecture

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

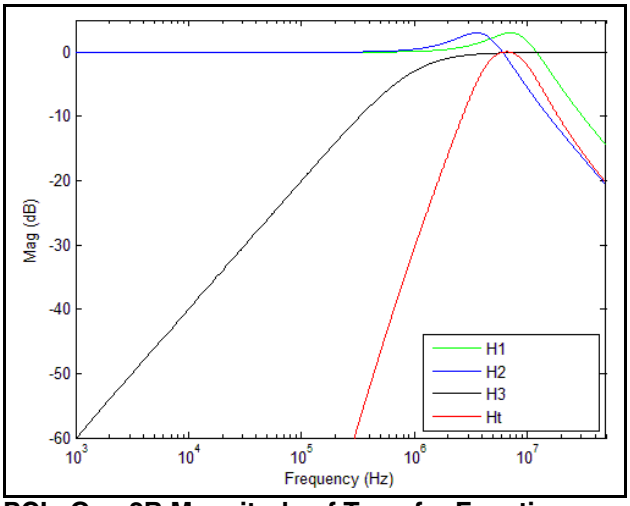


PCIe Gen 1 Magnitude of Transfer Function

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in RMS. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

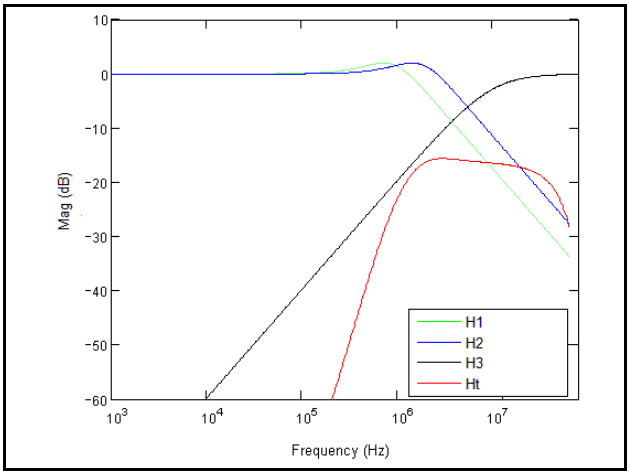


PCIe Gen 2A Magnitude of Transfer Function



PCIe Gen 2B Magnitude of Transfer Function

For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



PCIe Gen 3 Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements*.

LVPECL Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8T49N008I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8T49N008I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 225mA = **779.625mW**
- Power (outputs)$_{MAX}$ = **31.55mW/Loaded Output pair**
  If all outputs are loaded, the total power is 8 * 31.55mW = **252.4mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 779.625W + 252.4mW = **1032.025W**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 32.4°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.032W * 32.4°C/W = 118.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 40-Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**3**
Multi-Layer PCB, JEDEC Standard Test Boards	32.4°C/W	25.7°C/W	23.4°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 10.*

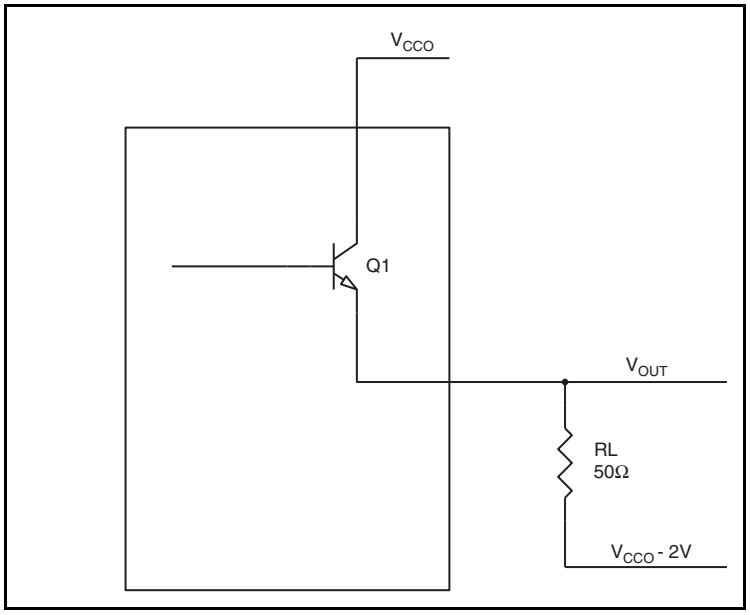


Figure 10. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC\ O}$ – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.75V}$
  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.75V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.6V}$
  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.6V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.75V)/50\Omega] * 0.75V =$ **18.75mW**

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.6V)/50\Omega] * 1.6V =$ **12.80mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **31.55mW**

LVDS Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8T49N008I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8T49N008I is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.3V +5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX} = V_{CC\_MAX} * (I_{CC\_MAX} + I_{CCA\_MAX}) = 3.465V * (125mA + 32mA) =$ **544.005mW**
- Power $(outputs)_{MAX} = V_{CCO\_MAX} * I_{CCO\_MAX} = 3.465V * 162mA =$ **561.33mW**

Total Power$_{\_MAX}$ = 544.005mW + 561.33mW = **1105.335mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 32.4°C/W per Table 8 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.105W * 32.4°C/W = 120.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 8. Thermal Resistance θ_{JA} for 40-Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.4°C/W	25.7°C/W	23.4°C/W

Reliability Information

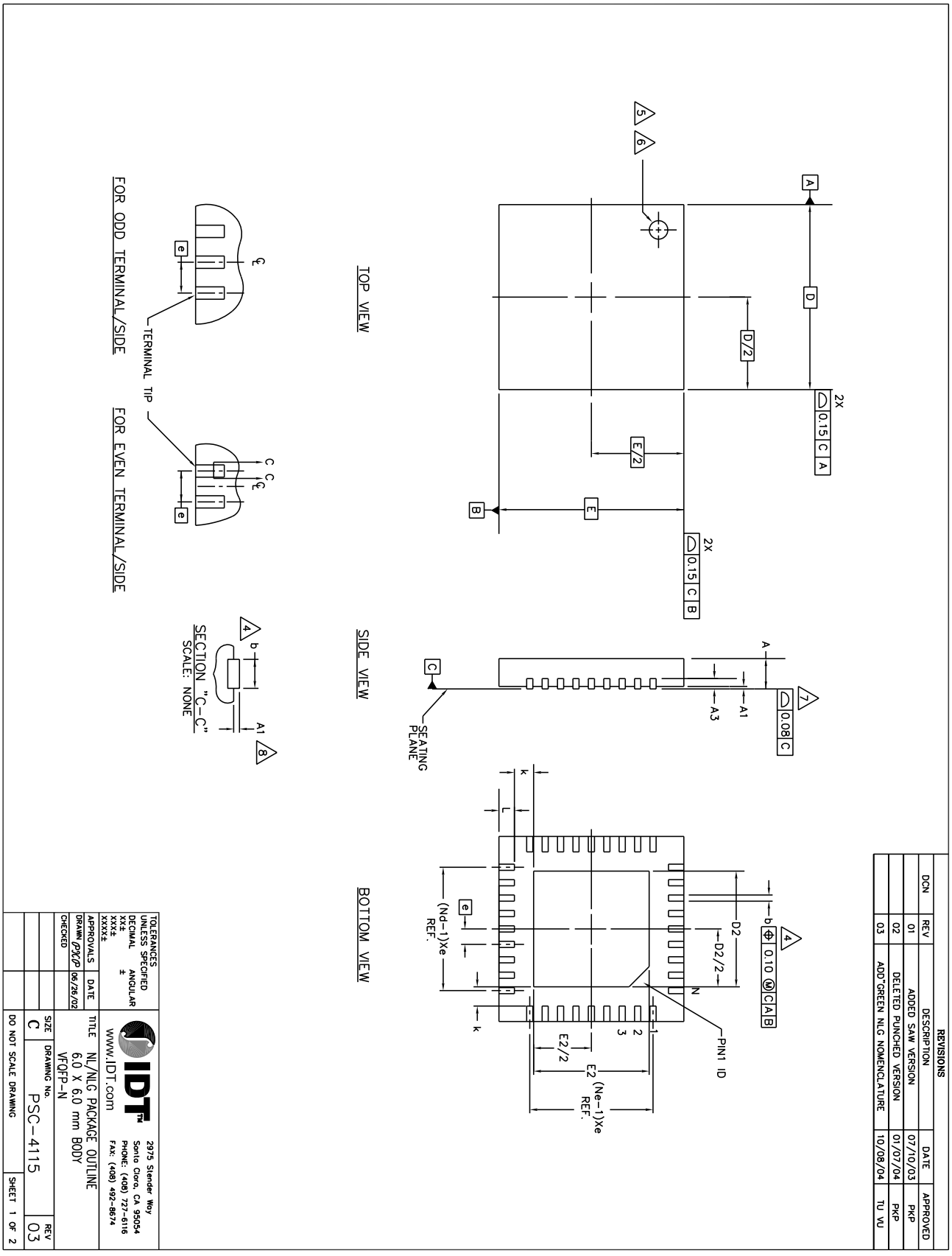
Table 9. θ_{JA} vs. Air Flow Table for a 40-Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.4°C/W	25.7°C/W	23.4°C/W

Transistor Count

The transistor count for IDT8T49N008I is: 26,856

40-Lead VFQFN Package Outline and Package Dimensions



40-Lead VFQFN Package Outline and Package Dimensions, continued

SYMBOL	JEDEC VARIATION VJJC-3			NOTE
	MIN.	NOM.	MAX.	
e		0.65 BSC		
N		28		
Nd		7		
Ne		7		
b	0.25	0.30	0.35	4
D2	–	10		
E2	–	10		

SYMBOL	JEDEC VARIATION VJJD-5			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		40		3
Nd		10		3
Ne		10		3
b	0.18	0.25	0.30	4
D2	–	–		10
E2	–	–		10

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	–	0.90	1.00	
A1	0.00	0.02	0.05	7
A3		0.20 REF.		
D		6.00 BSC		
E		6.00 BSC		
k	0.20	–	–	
L	0.35	0.40	0.45	

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
3. ALL DIMENSIONS ARE IN MILLIMETERS.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. APPLIED TO EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY FOR TERMINALS.
9. THIS OUTLINES CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-220, VARIATION VJJC-3 & VJJD-5 WITH THE EXCEPTION OF D2 & E2.
10. DIMENSIONS D2 & E2 VARY DEPENDING ON DEVICE, SUPPLIER, ETC.

40-Lead VFQFN, D2/E2 EPAD Dimensions: 4.65mm x 4.65mm

REVISIONS			
DCN	REV	DESCRIPTION	DATE	APPROVED
	01	ADDED SAW VERSION	07/10/03	PKP
	02	DELETED PUNCHED VERSION	01/07/04	PKP
	03	ADD"GREEN" NLG NOMENCLTURE	10/08/04	TU VU

TOLERANCES UNLESS SPECIFIED		IDT™	2975 Stender Way Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674
DECIMAL ANGULAR ±		WWW.IDT.com	
XX± XXX± XXXX±		TITLE NL/NLG PACKAGE OUTLINE 6.0 X 6.0 mm BODY VFQFP-N	
APPROVALS	DATE		
DRAWN PJX/P	06/25/02		
CHECKED		SIZE C	DRAWING No. PSC-4115	REV 03
DO NOT SCALE DRAWING			SHEET 2 OF 2

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T49N008A-dddNLGI	IDT8T49N008A-dddNLGI	“Lead-Free” 40-Lead VFQFN	Tray	-40°C to 85°C
8T49N008A-dddNLGI8	IDT8T49N008A-dddNLGI	“Lead-Free” 40-Lead VFQFN	Tape & Reel	-40°C to 85°C

NOTE: For the specific -ddd order codes, refer to the *Programmable FemtoClock® NG Product Ordering Guide* document.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		1	Pin Assignment - repositioned pin numbers (11-20).	4/18/12
A	T10	36	Changed footer part/order number from IDT8T49N008BNLGI to IDT8T49N008ANLGI. Ordering Information Table - changed Shipping Packaging from 1000 Tape & Reel to 5000 Tape & Reel.	4/23/12
A	 T10	11, 38 38	Changed name of the *IDT8T49N00xI Programmable FemtoClock® NG Product Ordering Information* document to *Programmable FemtoClock® Ordering Product Information* Deleted quantity from Tape & Reel, Deleted Lead Free note.	8/21/13
A	 T10	1 11 38	Changed title to Programmable FemtoClock® NG LVPECL/LVDS Clock Generator with 8-Outputs. Changed text from '*Programmable FemtoClock® Ordering Product Information'* to '*Programmable FemtoClock® NG Product Ordering Guide'.* Changed Note from '*Programmable FemtoClock® Ordering Product Information'* to '*Programmable FemtoClock® NG Product Ordering Guide'.*	9/26/13
A	T5	14	Changed the min load capacitance from 12pF to 10pF	10/15/13
A			Corrected part number in the footer pages from IDT8T49N00BNLGI to IDT8T49N00ANLGI	2/13/14

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