

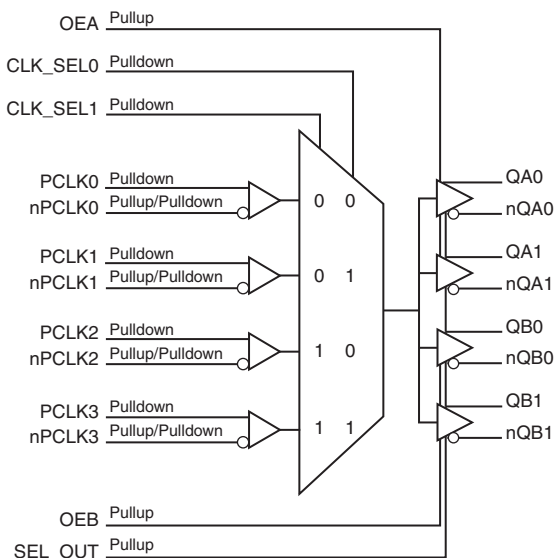
### General Description

The ICS859S0424I is a 4:4 Differential-to-LVPECL/ LVDS Clock Multiplexer which can operate up to 3GHz. The outputs for this device can either be programmed to give LVPECL or LVDS levels. The ICS859S0424I has four selectable differential PCLKx, nPCLKx clock inputs. The PCLKx, nPCLKx input pairs can accept LVPECL, LVDS or CML levels. The fully differential architecture and low propagation delay make it ideal for use in clock distribution circuits.

### Features

- High speed 4:1 differential multiplexer with a 1:4 fanout buffer
- Four programmable differential LVPECL or LVDS output pairs
- Four selectable differential PCLKx, nPCLKx input pairs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML
- Maximum output frequency: 3GHz
- Translates any single ended input signal to LVPECL levels with resistor bias on nPCLKx inputs
- Part-to-part skew: 100ps (maximum)
- Propagation delay: 555ps (typical) @ 3.3V
- Additive phase jitter, RMS: 0.22ps (typical) @ 3.3V
- Full 3.3V or 2.5V supply modes
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

### Block Diagram



### Pin Assignment

CLK_SEL0	1	24	Vcc
CLK_SEL1	2	23	VEE
PCLK0	3	22	QA0
nPCLK0	4	21	nQA0
PCLK1	5	20	QA1
nPCLK1	6	19	nQA1
PCLK2	7	18	QB0
nPCLK2	8	17	nQB0
PCLK3	9	16	QB1
nPCLK3	10	15	nQB1
OEA	11	14	VCC_TAP
OEB	12	13	SEL_OUT

**ICS859S0424I**

**24-Lead TSSOP**

**4.4mm x 7.8mm x 0.925mm package body**

**G Package**

**Top View**

**Table 2. Pin Descriptions**

Number	Name	Type		Description
1, 2	CLK_SEL0, CLK_SEL1	Input	Pulldown	Clock select inputs. See Table 4A. LVCMOS / LVTTTL interface levels.
3	PCLK0	Input	Pulldown	Non-inverting differential LVPECL clock input.
4	nPCLK0	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{CC}/2$ default when left floating.
5	PCLK1	Input	Pulldown	Non-inverting differential clock input.
6	nPCLK1	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{CC}/2$ default when left floating.
7	PCLK2	Input	Pulldown	Non-inverting differential clock input.
8	nPCLK2	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{CC}/2$ default when left floating.
9	PCLK3	Input	Pulldown	Non-inverting differential clock input.
10	nPCLK3	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{CC}/2$ default when left floating.
11	OEA	Input	Pullup	Output enable pin for Bank A outputs. See Table 4B. LVCMOS/LVTTTL interface levels.
12	OEB	Input	Pullup	Output enable pin for Bank B outputs. See Table 4B. LVCMOS/LVTTTL interface levels.
13	SEL_OUT	Input	Pullup	Output select pin. When LOW, selects LVDS levels. When HIGH, selects LVPECL levels. LVCMOS/LVTTTL interface levels. See Table 1B.
14	$V_{CC\_TAP}$	Power		Power supply pin. See Table 1A.
15, 16	nQB1, QB1	Output		Differential output pair. LVPECL or LVDS interface levels.
17, 18	nQB0, QB0	Output		Differential output pair. LVPECL or LVDS interface levels.
19, 20	nQA1, QA1	Output		Differential output pair. LVPECL or LVDS interface levels.
21, 22	nQA0, QA0	Output		Differential output pair. LVPECL or LVDS interface levels.
23	$V_{EE}$	Power		Negative supply pin.
24	$V_{CC}$	Power		Power supply pin.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 3. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$C_{IN}$	Input Capacitance			2		pF
$R_{PULLUP}$	Input Pullup Resistor			51		k $\Omega$
$R_{PULLDOWN}$	Input Pulldown Resistor			51		k $\Omega$
$R_{VCC/2}$	Input Pullup/Pulldown Resistor			50		k $\Omega$

## Function Tables

**Table 4A. Clock Input Function Table**

Inputs		Outputs
CLK_SEL1	CLK_SEL0	Qx[0:1], nQx[0:1]
0	0	PCLK0, nPCLK0 (default)
0	1	PCLK1, nPCLK1
1	0	PCLK2, nPCLK2
1	1	PCLK3, nPCLK3

**Table 4B. V<sub>CC\_TAP</sub> Function Table**

Outputs	Output Level Supply	V <sub>CC_TAP</sub>
Qx[0:1], nQx[0:1]		
LVPECL	2.5V	V <sub>CC</sub>
LVPECL	3.3V	V <sub>CC</sub>
LVDS	2.5V	V <sub>CC</sub>
LVDS	3.3V	Float

**Table 4C. SEL\_OUT Function Table**

Input	Outputs
SEL_OUT	Qx[0:1], nQx[0:1]
1	LVPECL (default)
0	LVDS

**Table 4D. Output Enable Function Table**

Inputs	Outputs
OEA, OEB	Qx[0:1], nQx[0:1]
0	Low/High
1	Normal Operation (default)

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_O$ (LVPECL) Continuous Current Surge Current	50mA 100mA
Outputs, $I_O$ (LVDS) Continuous Current Surge Current	10mA 15mA
Package Thermal Impedance, $\theta_{JA}$	82.8°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 5A. LVPECL Power Supply DC Characteristics,  $V_{CC} = V_{CC\_TAP} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Power Supply Voltage		3.135	3.3	3.465	V
$V_{CC\_TAP}$	Power Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current				72	mA
$I_{CC\_TAP}$	Power Supply Current				5	mA

**Table 5B. LVPECL Power Supply DC Characteristics,  $V_{CC} = V_{CC\_TAP} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Power Supply Voltage		2.375	2.5	2.625	V
$V_{CC\_TAP}$	Power Supply Voltage		2.375	2.5	2.625	V
$I_{EE}$	Power Supply Current				66	mA
$I_{CC\_TAP}$	Power Supply Current				5	mA

**Table 5C. LVDS Power Supply DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Positive Supply Voltage		3.135	3.3	3.465	V
$I_{CC}$	Power Supply Current				140	mA
$I_{CC\_TAP}$	Power Supply Current				5	mA

**Table 5D. LVDS Power Supply DC Characteristics,  $V_{CC} = V_{CC\_TAP} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Positive Supply Voltage		2.375	2.5	2.625	V
$V_{CC\_TAP}$	Positive Supply Voltage		2.375	2.5	2.625	V
$I_{CC}$	Power Supply Current				130	mA
$I_{CC\_TAP}$	Power Supply Current				5	mA

**Table 5E. LVCMOS/LVTTL DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		$V_{CC} = 3.465V$	2.2		$V_{CC} + 0.3$	V
			$V_{CC} = 2.625V$	1.7		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage		$V_{CC} = 3.465V$	-0.3		0.8	V
			$V_{CC} = 2.625V$	-0.3		0.7	V
$I_{IH}$	Input High Current	CLK_SEL0, CLK_SEL1	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$			150	$\mu A$
		OEA, OEB, SEL_OUT	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$			10	$\mu A$
$I_{IL}$	Input Low Current	CLK_SEL0, CLK_SEL1	$V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-10			$\mu A$
		OEA, OEB, SEL_OUT	$V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-150			$\mu A$

**Table 5F. LVPECL DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	PCLK0, nPCLK0, PCLK1, nPCLK1	$V_{CC} = V_{IN} = 3.465V$			150	$\mu A$
$I_{IL}$	Input Low Current	PCLK0, PCLK1	$V_{CC} = 3.465V$ , $V_{IN} = 0V$	-10			$\mu A$
		nPCLK0, nPCLK1	$V_{CC} = 3.465V$ , $V_{IN} = 0V$	-150			$\mu A$
$V_{PP}$	Peak-to-Peak Voltage			0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1			1.2		$V_{CC}$	V
$V_{OH}$	Output High Voltage; NOTE 2			$V_{CC} - 1.4$		$V_{CC} - 0.9$	V
$V_{OL}$	Output Low Voltage; NOTE 2			$V_{CC} - 2.0$		$V_{CC} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing			0.6		1.0	V

NOTE 1: Common mode input voltage is defined as  $V_{IH}$ .NOTE 2: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .**Table 5G. LVPECL DC Characteristics,  $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	PCLK0, nPCLK0, PCLK1, nPCLK1	$V_{CC} = V_{IN} = 2.625V$			150	$\mu A$
$I_{IL}$	Input Low Current	PCLK0, PCLK1	$V_{CC} = 2.625V$ , $V_{IN} = 0V$	-10			$\mu A$
		nPCLK0, nPCLK1	$V_{CC} = 2.625V$ , $V_{IN} = 0V$	-150			$\mu A$
$V_{PP}$	Peak-to-Peak Voltage			0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1			1.2		$V_{CC}$	V
$V_{OH}$	Output High Voltage; NOTE 2			$V_{CC} - 1.4$		$V_{CC} - 0.9$	V
$V_{OL}$	Output Low Voltage; NOTE 2			$V_{CC} - 2.0$		$V_{CC} - 1.5$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing			0.4		1.0	V

NOTE 1: Common mode input voltage is defined as  $V_{IH}$ .NOTE 2: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

**Table 5H. LVDS DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage	SEL_OUT = 0	247		454	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change	SEL_OUT = 0			50	mV
$V_{OS}$	Offset Voltage	SEL_OUT = 0	1.10		1.40	V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change	SEL_OUT = 0			50	mV

**Table 5I. LVDS DC Characteristics,  $V_{CC} = V_{CC\_TAP} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage	SEL_OUT = 0	247		454	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change	SEL_OUT = 0			50	mV
$V_{OS}$	Offset Voltage	SEL_OUT = 0	1.10		1.40	V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change	SEL_OUT = 0			50	mV

## AC Electrical Characteristics

**Table 6A. LVPECL AC Characteristics,  $V_{CC} = V_{CC\_TAP} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency				3	GHz
$t_{PD}$	Propagation Delay; NOTE 1		400		800	ps
$f_{jit}$	Buffer Additive Phase Jitter, RMS; NOTE 2	100MHz, Integration Range: 12kHz – 20MHz		0.22	0.28	ps
$t_{sk(b)}$	Bank Skew; NOTE 3, 4				25	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 4, 5				100	ps
$t_{sk(o)}$	Output Skew; NOTE 4, 6				25	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	50		245	ps
odc	Output Duty Cycle		46		54	%
$MUX_{ISOLATION}$	MUX Isolation	$f_{OUT} < 1.2\text{GHz}$		45		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters are measured at  $f_{OUT} \leq 1.5\text{GHz}$ , unless otherwise noted.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Measured on Agilent E5052A Signal Source Analyzer. Refer to Additive Phase Jitter section.

NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.

NOTE 4: These parameters are guaranteed by characterization. Not tested in production.

NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at the differential cross points.

NOTE 6: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

**Table 6B. LVPECL AC Characteristics,  $V_{CC} = V_{CC\_TAP} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency				3	GHz
$t_{PD}$	Propagation Delay; NOTE 1		400		800	ps
$f_{jit}$	Buffer Additive Phase Jitter, RMS; NOTE 2	100MHz, Integration Range: 12kHz – 20MHz		0.22	0.28	ps
$t_{sk(b)}$	Bank Skew; NOTE 3, 4				25	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 4, 5				100	ps
$t_{sk(o)}$	Output Skew; NOTE 4, 6				25	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	50		235	ps
odc	Output Duty Cycle		46		54	%
$MUX_{ISOLATION}$	MUX Isolation	$f_{OUT} < 1.2\text{GHz}$		45		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters are measured at  $f_{OUT} \leq 1.5\text{GHz}$ , unless otherwise noted.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Measured on Agilent E5052A Signal Source Analyzer. Refer to Additive Phase Jitter section.

NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.

NOTE 4: These parameters are guaranteed by characterization. Not tested in production.

NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at the differential cross points.

NOTE 6: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

**Table 6C. LVDS AC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency				3	GHz
$t_{PD}$	Propagation Delay; NOTE 1		400		800	ps
$\tau_{jit}$	Buffer Additive Phase Jitter, RMS; NOTE 2	100MHz, Integration Range: 12kHz – 20MHz		0.26	0.30	ps
$\tau_{sk(b)}$	Bank Skew; NOTE 3, 4				25	ps
$\tau_{sk(pp)}$	Part-to-Part Skew; NOTE 4, 5				100	ps
$\tau_{sk(o)}$	Output Skew; NOTE 4, 6				25	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	50		200	ps
odc	Output Duty Cycle		46		54	%
$MUX_{ISOLATION}$	MUX Isolation	$f_{OUT} < 1.2\text{GHz}$		45		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters are measured at  $f_{OUT} \leq 1.5\text{GHz}$ , unless otherwise noted.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Measured on Agilent E5052A Signal Source Analyzer. Refer to Additive Phase Jitter section.

NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.

NOTE 4: These parameters are guaranteed by characterization. Not tested in production.

NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at the differential cross points.

NOTE 6: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

**Table 6D. LVDS AC Characteristics,  $V_{CC} = V_{CC\_TAP} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency				3	GHz
$t_{PD}$	Propagation Delay; NOTE 1		400		800	ps
$\tau_{jit}$	Buffer Additive Phase Jitter, RMS; NOTE 2	100MHz, Integration Range: 12kHz – 20MHz		0.26	0.31	ps
$\tau_{sk(b)}$	Bank Skew; NOTE 3, 4				25	ps
$\tau_{sk(pp)}$	Part-to-Part Skew; NOTE 4, 5				100	ps
$\tau_{sk(o)}$	Output Skew; NOTE 4, 6				25	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	50		200	ps
odc	Output Duty Cycle		46		54	%
$MUX_{ISOLATION}$	MUX Isolation	$f_{OUT} < 1.2\text{GHz}$		45		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters are measured at  $f_{OUT} \leq 1.5\text{GHz}$ , unless otherwise noted.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Measured on Agilent E5052A Signal Source Analyzer. Refer to Additive Phase Jitter section.

NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.

NOTE 4: These parameters are guaranteed by characterization. Not tested in production.

NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at the differential cross points.

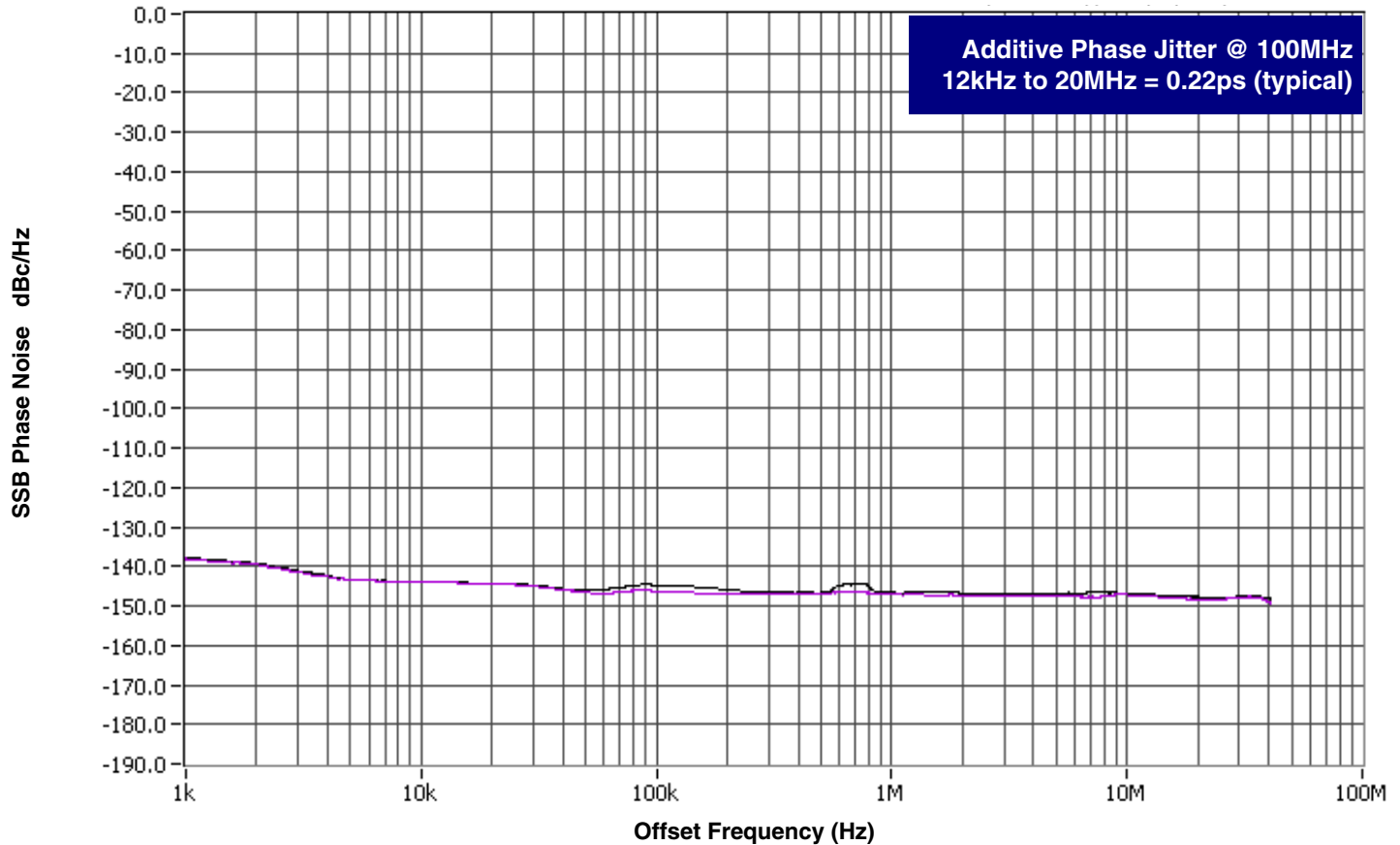
NOTE 6: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.



## Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise***. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

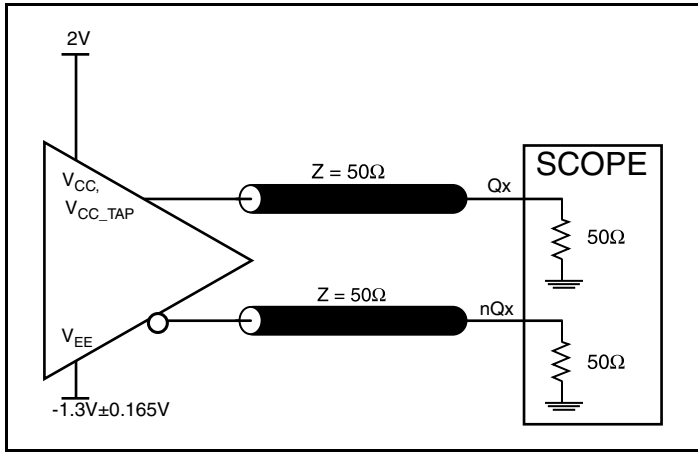


As with most timing specifications, phase noise measurements have issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is

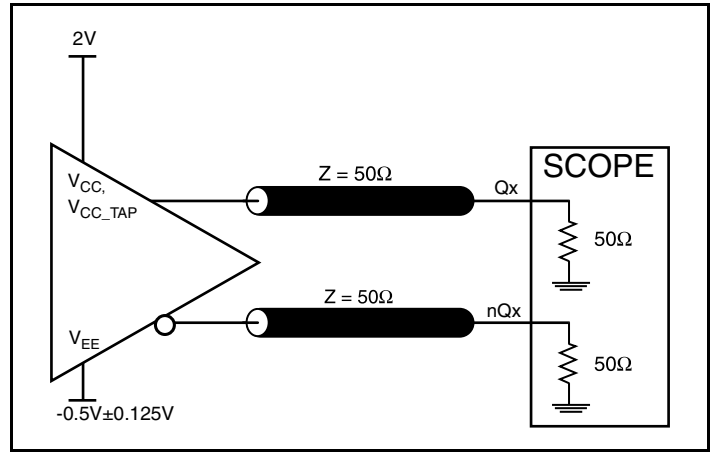
shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Measured using a Rohde & Schwarz SMA100 as the input source.

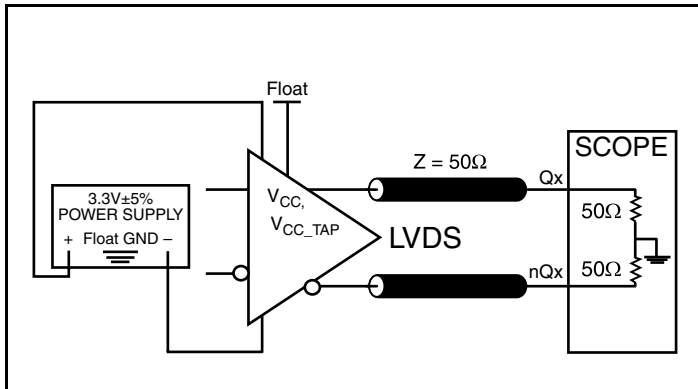
### Parameter Measurement Information



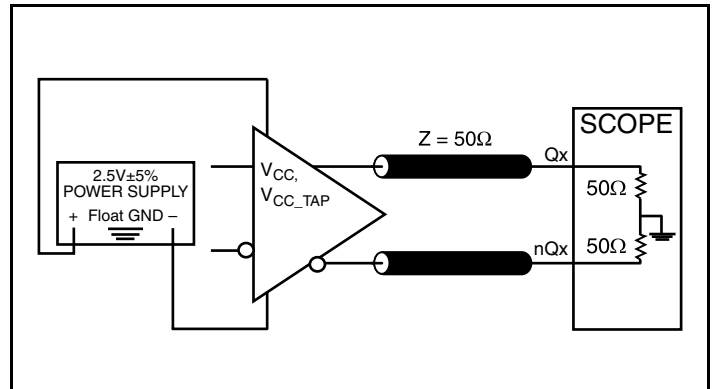
3.3V LVPECL Output Load AC Test Circuit



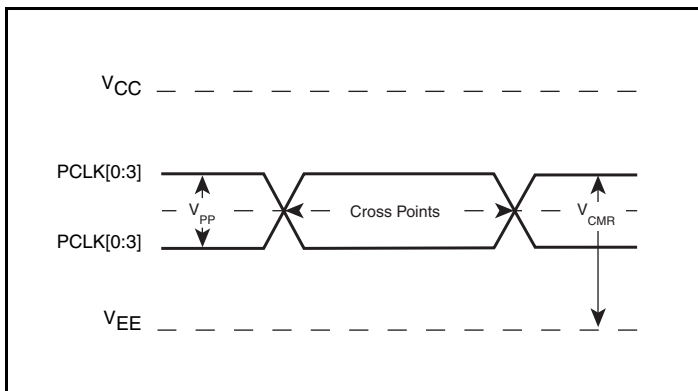
2.5V LVPECL Output Load AC Test Circuit



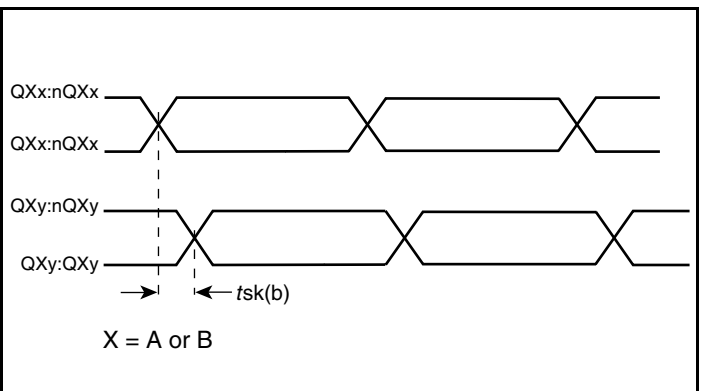
3.3V LVDS Output Load AC Test Circuit



2.5V LVDS Output Load AC Test Circuit

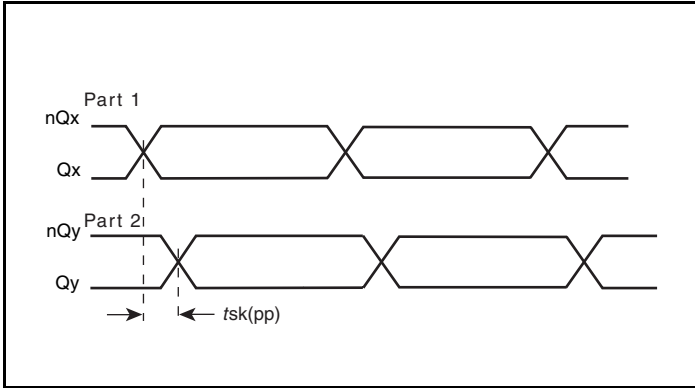


Differential Input Level

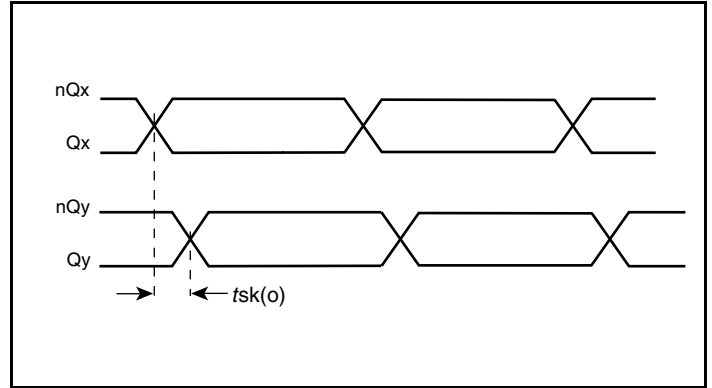


Bank Skew

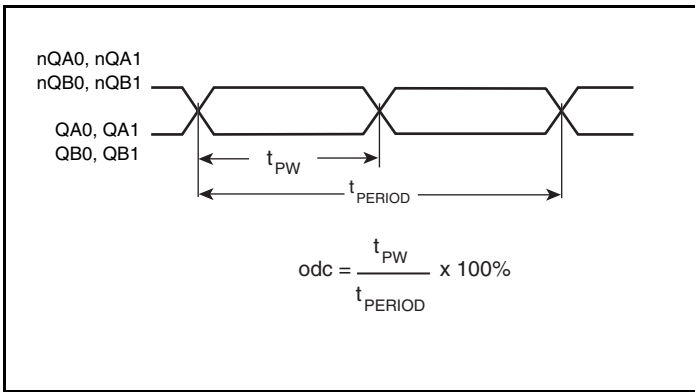
### Parameter Measurement Information, continued



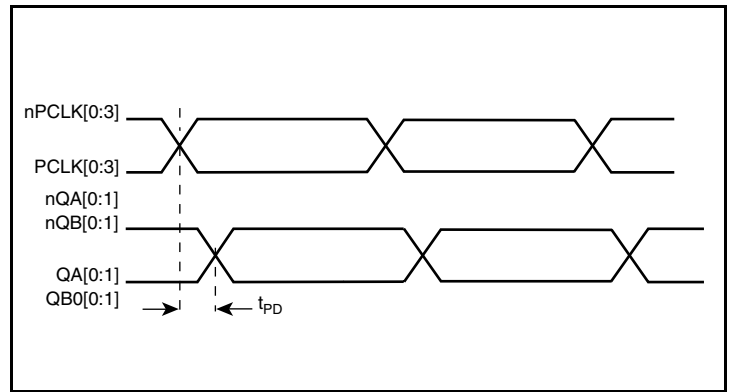
**Part-to-Part Skew**



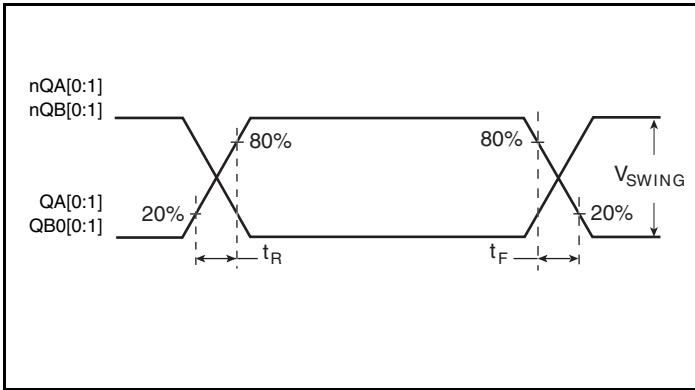
**Output Skew**



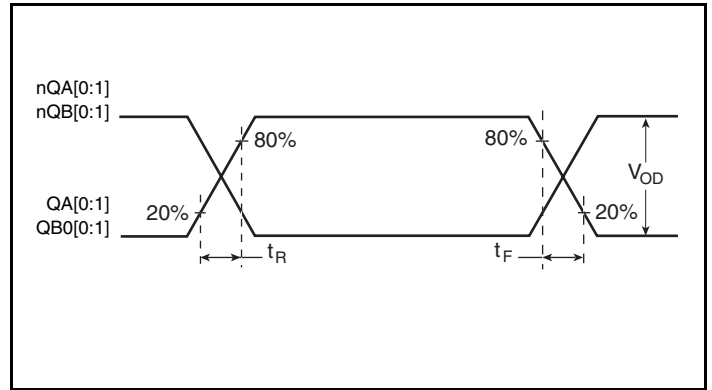
**Output Duty Cycle/Pulse Width/Period**



**Propagation Delay**

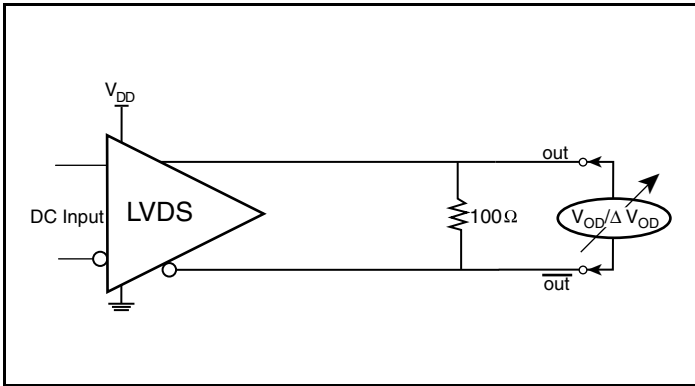


**LVPECL Output Rise/Fall Time**

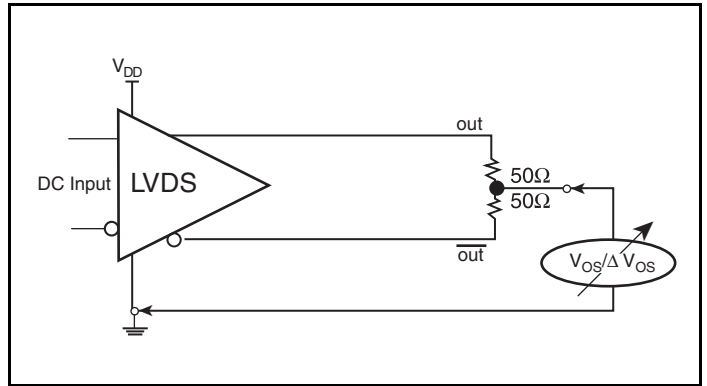


**LVDS Output Rise/Fall Time**

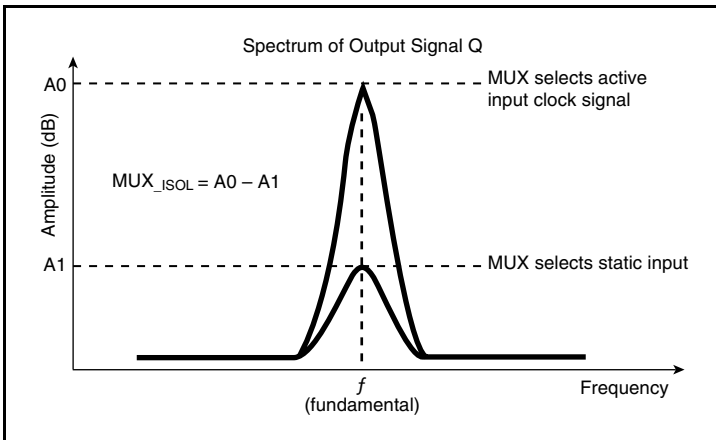
### Parameter Measurement Information, continued



Differential Output Voltage Setup



Offset Voltage Setup



MUX Isolation

## Applications Information

### Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{CC}/2$  is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is 2.5V and  $V_{CC} = 3.3V$ , R1 and R2 value should be adjusted to set  $V_{REF}$  at 1.25V. The values below are for when both the single ended swing and  $V_{CC}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission

line impedance. For most 50 $\Omega$  applications, R3 and R4 can be 100 $\Omega$ . The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than -0.3V and  $V_{IH}$  cannot be more than  $V_{CC} + 0.3V$ . Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

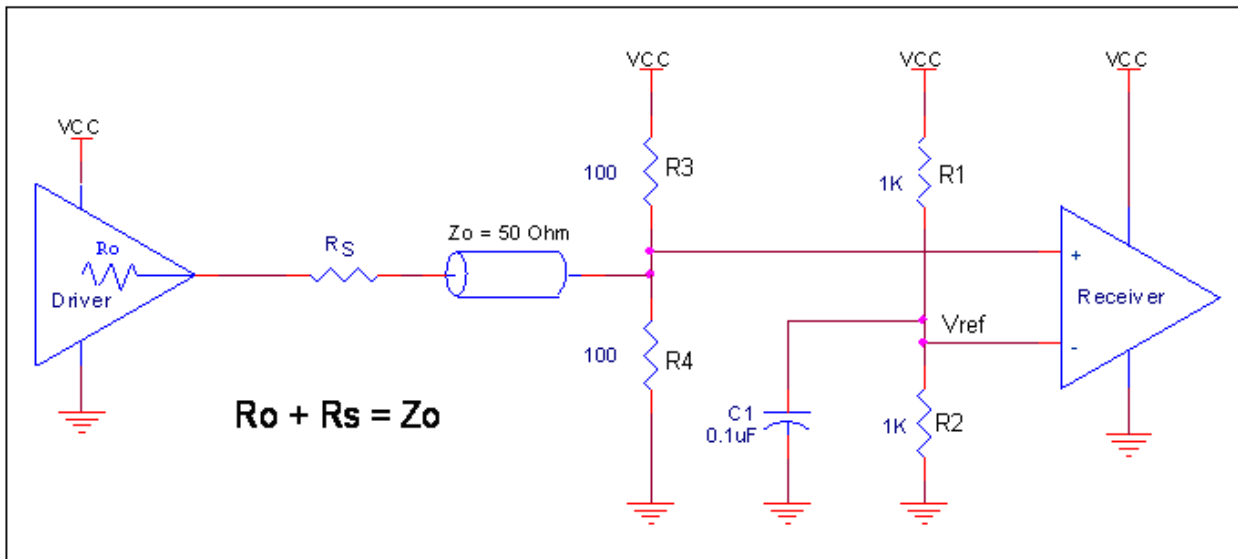


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

### 3.3V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, CML and other differential signals. Both signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 2A to 2E show interface examples for the PCLK/ nPCLK input driven by the most common driver types. The

input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

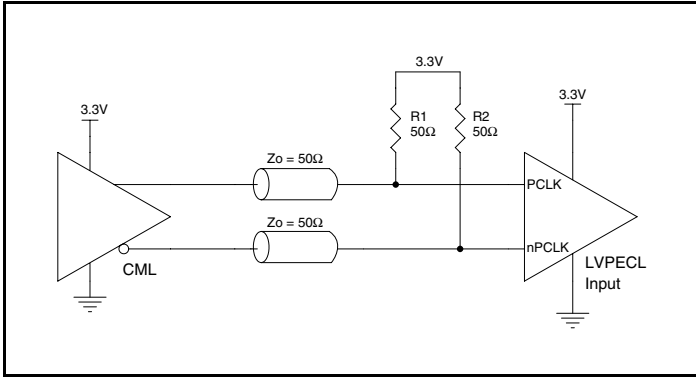


Figure 2A. PCLK/nPCLK Input Driven by a CML Driver

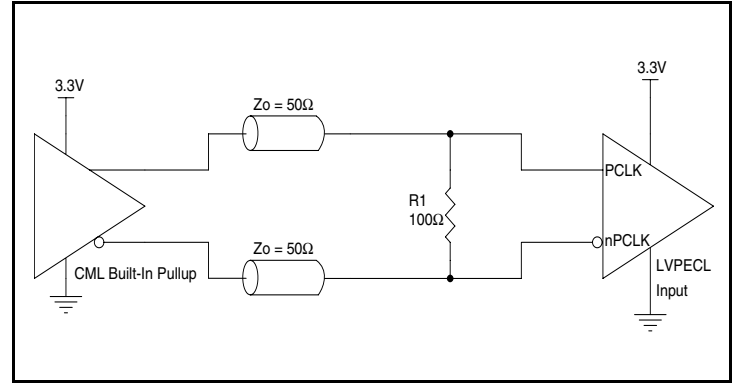


Figure 2B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

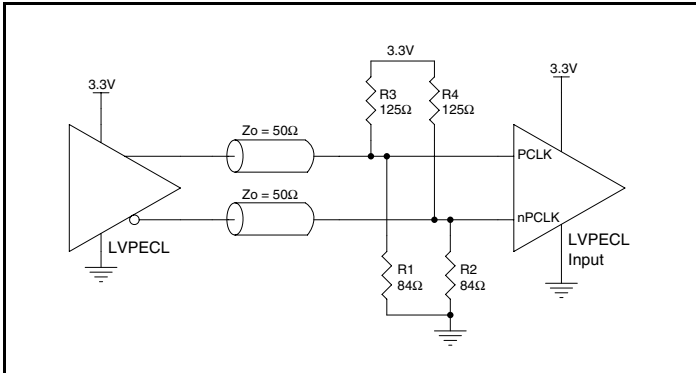


Figure 2C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

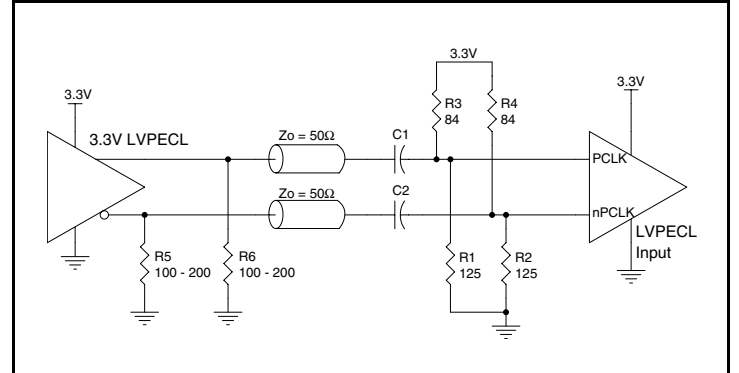


Figure 2D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

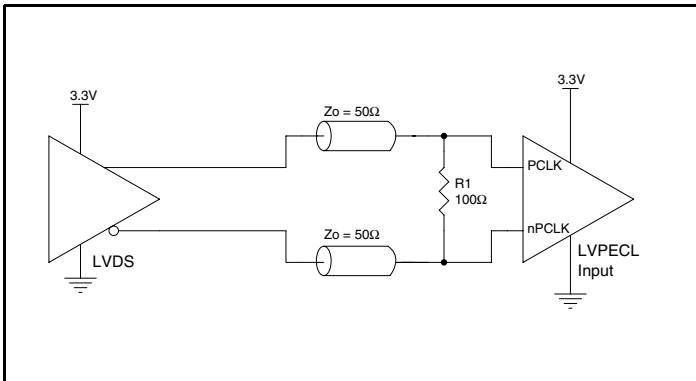
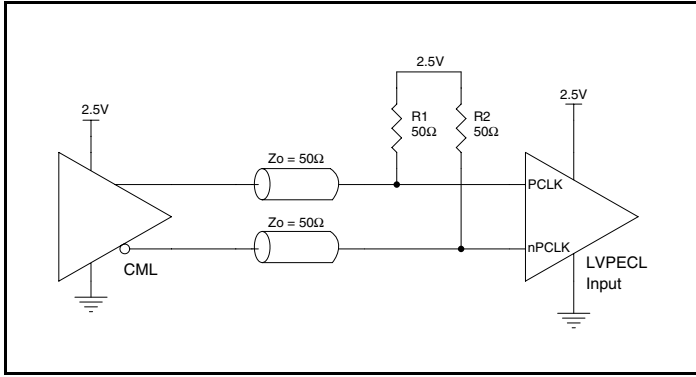


Figure 2E. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

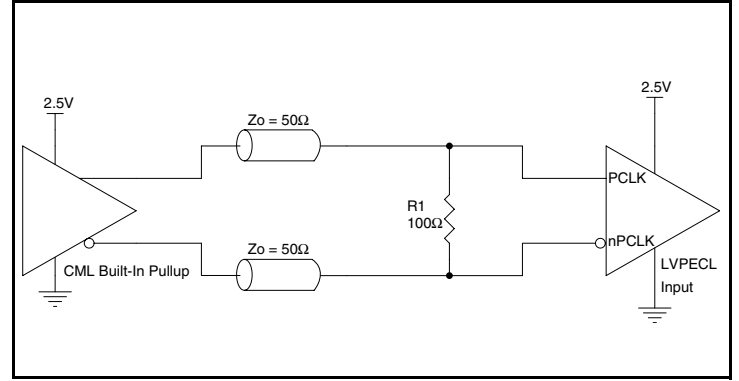
## 2.5V LVPECL Clock Input Interface

The PCLK/nPCLK accepts LVPECL, LVDS, CML and other differential signals. Both signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. *Figures 3A to 3E* show interface examples for the PCLK/nPCLK input driven by the most common driver types. The

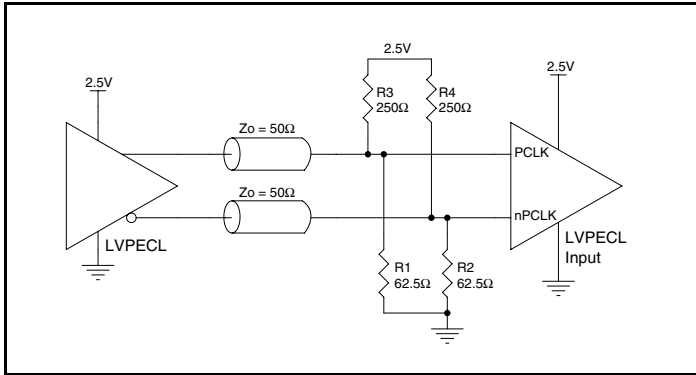
input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



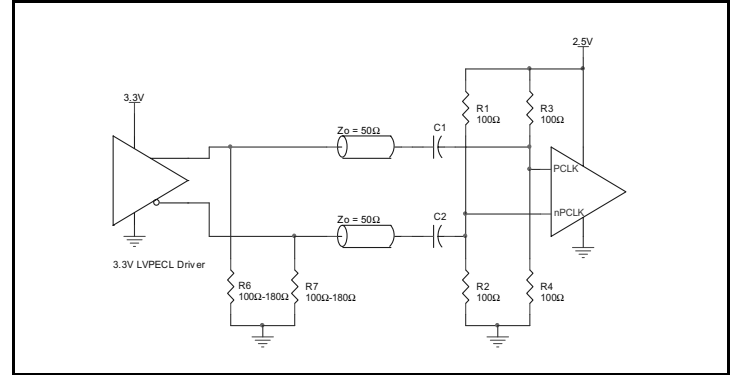
**Figure 3A. PCLK/nPCLK Input Driven by a CML Driver**



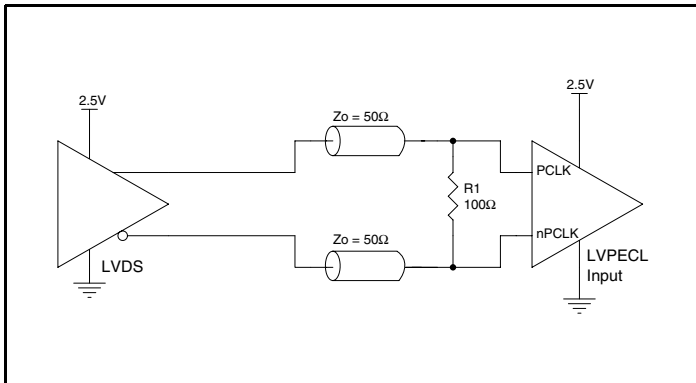
**Figure 3B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver**



**Figure 3C. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver**



**Figure 3D. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver with AC Couple**



**Figure 3E. PCLK/nPCLK Input Driven by a 2.5V LVDS Driver**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### PCLK/nPCLK Inputs

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from PCLK to ground.

#### LVC MOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A  $1\text{k}\Omega$  resistor can be used.

### Outputs:

#### LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

#### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with  $100\Omega$  across. If they are left floating, there should be no trace attached.

## Termination for 2.5V LVPECL Outputs

Figure 4A and Figure 4B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating  $50\Omega$  to  $V_{CC} - 2V$ . For  $V_{CC} = 2.5V$ , the  $V_{CC} - 2V$  is very close to ground.

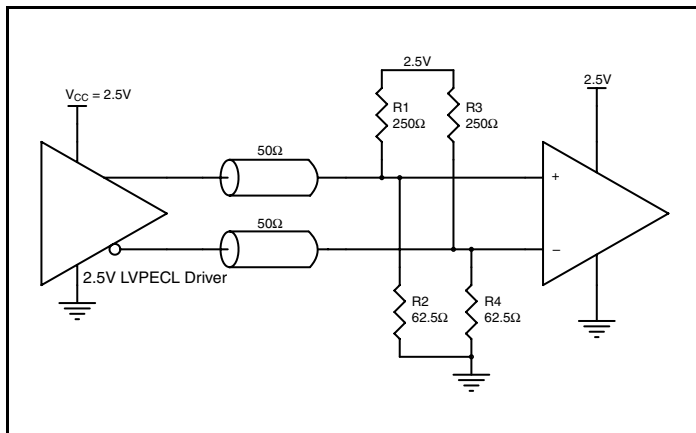


Figure 4A. 2.5V LVPECL Driver Termination Example

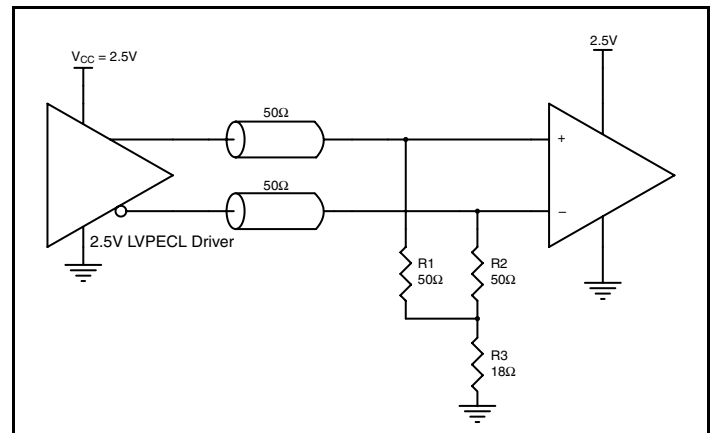


Figure 4B. 2.5V LVPECL Driver Termination Example

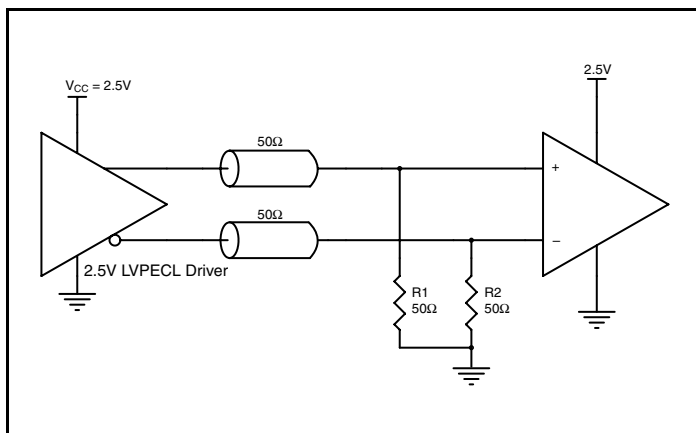


Figure 4C. 2.5V LVPECL Driver Termination Example

level. The R3 in Figure 4B can be eliminated and the termination is shown in Figure 4C.



## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

*Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

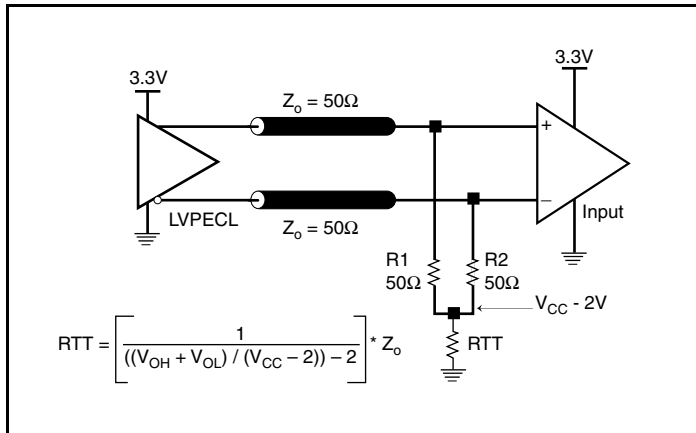


Figure 5A. 3.3V LVPECL Output Termination

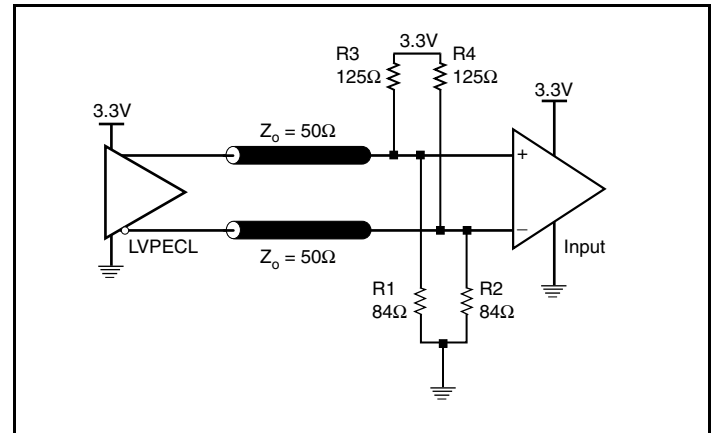
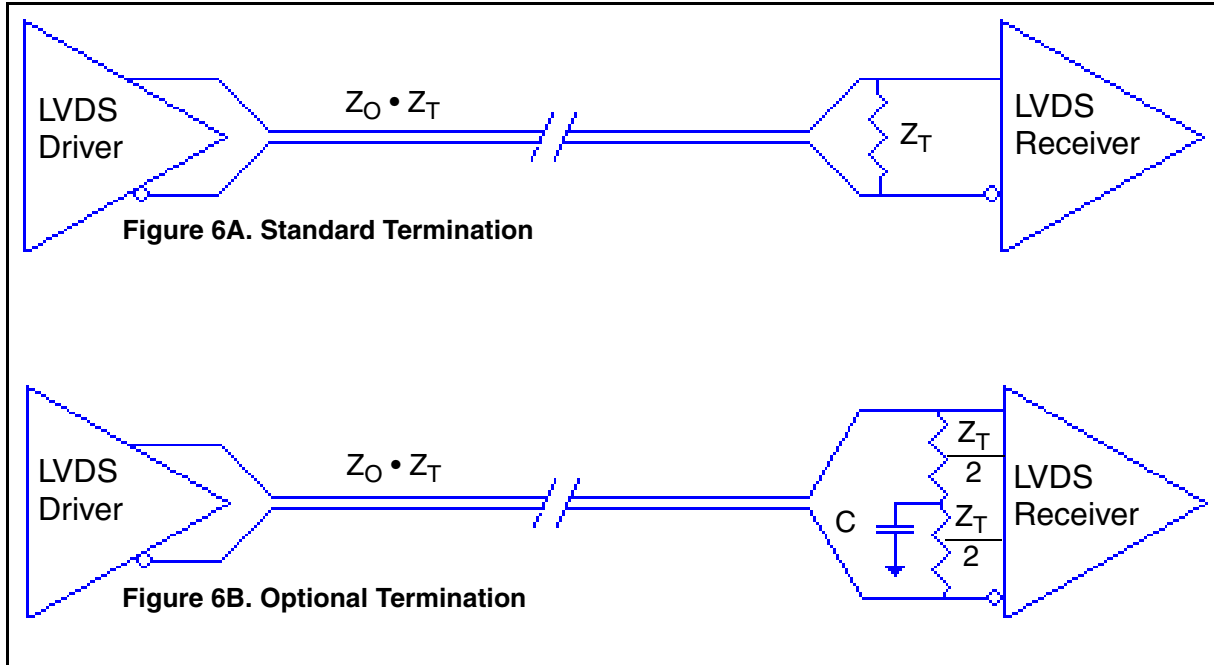


Figure 5B. 3.3V LVPECL Output Termination

## LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance ( $Z_T$ ) is between  $90\Omega$  and  $132\Omega$ . The actual value should be selected to match the differential impedance ( $Z_0$ ) of your transmission line. A typical point-to-point LVDS design uses a  $100\Omega$  parallel resistor at the receiver and a  $100\Omega$  differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The

standard termination schematic as shown in *Figure 6A* can be used with either type of output structure. *Figure 6B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately  $50\text{pF}$ . If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.



### LVDS Termination

## Power Considerations (3.3V LVPECL Outputs)

This section provides information on power dissipation and junction temperature for the ICS859S0424I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS859S0424I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 72mA = 249.5mW$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $4 * 30mW = 120mW$

**Total Power**<sub>MAX</sub> (3.465V, with all outputs switching) =  $249.5mW + 120mW = 369.5mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 82.8°C/W per Table 7A below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.370W * 82.8^\circ C/W = 115.6^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

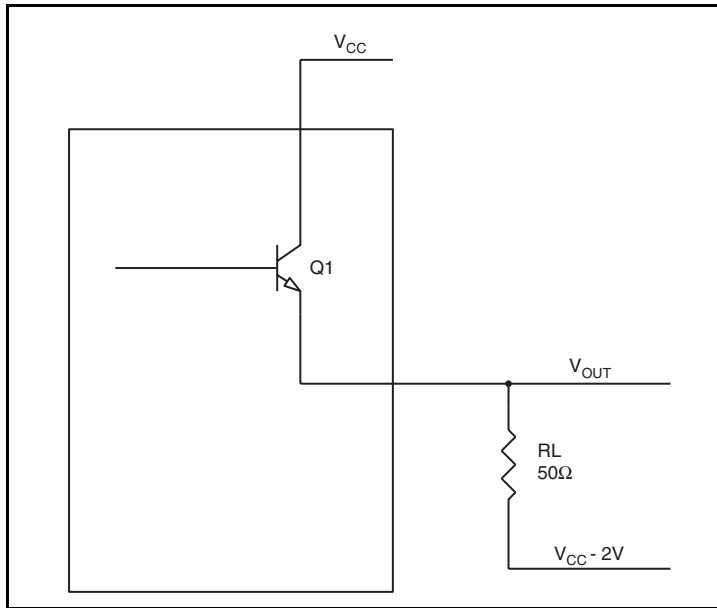
**Table 7A. Thermal Resistance  $\theta_{JA}$  for 24 Lead TSSOP, Forced Convection**

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	82.8°C/W	78.5	76.3

### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 7*.



**Figure 7. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V<sub>CC</sub> - 2V.

- For logic high, V<sub>OUT</sub> = V<sub>OH\_MAX</sub> = V<sub>CC\_MAX</sub> - 0.9V  
(V<sub>CC\_MAX</sub> - V<sub>OH\_MAX</sub>) = 0.9V
- For logic low, V<sub>OUT</sub> = V<sub>OL\_MAX</sub> = V<sub>CC\_MAX</sub> - 1.7V  
(V<sub>CC\_MAX</sub> - V<sub>OL\_MAX</sub>) = 1.7V

Pd<sub>H</sub> is power dissipation when the output drives high.

Pd<sub>L</sub> is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$$

$$Pd_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$$

Total Power Dissipation per output pair = Pd<sub>H</sub> + Pd<sub>L</sub> = **30mW**

## Power Considerations (3.3V LVDS Outputs)

This section provides information on power dissipation and junction temperature for the ICS859S0424I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS859S0424I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * I_{CC\_MAX} = 3.465V * 120mA = 415.8mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd_{total} + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd_{total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 82.8°C/W per Table 7B below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.416\text{W} * 82.8^\circ\text{C/W} = 119.4^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 7B. Thermal Resistance  $\theta_{JA}$  for 24 Lead TSSOP, Forced Convection**

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	82.8°C/W	78.5	76.3

## Reliability Information

Table 8.  $\theta_{JA}$  vs. Air Flow Table for a 24 Lead TSSOP

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	82.8°C/W	78.5	76.3

## Transistor Count

The transistor count for ICS859S0424I is: 585

## Package Outline and Package Dimensions

Package Outline - G Suffix for 24 Lead TSSOP

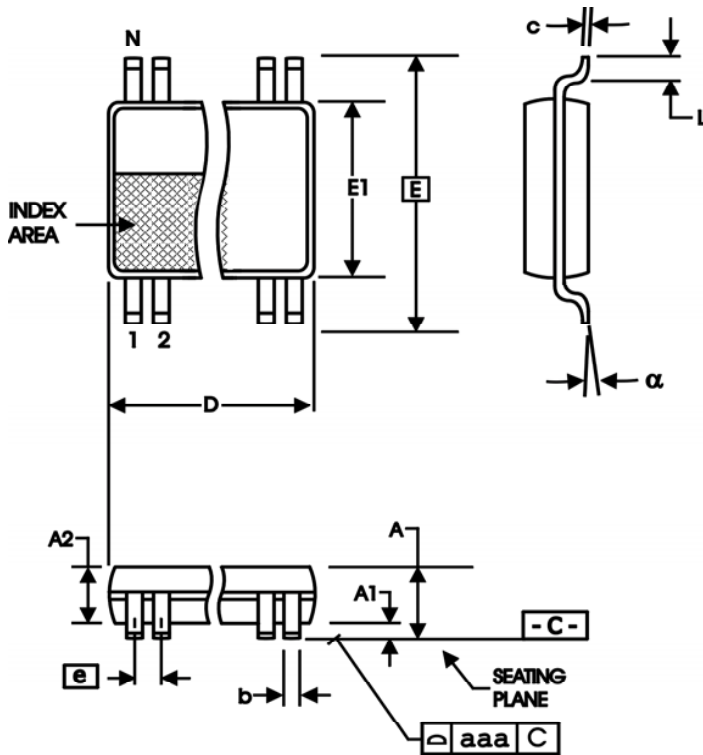


Table 9. Package Dimensions

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	24	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

## Ordering Information

**Table 10. Ordering Information**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
859S0424BGILF	ICS59S0424BIL	"Lead-Free" 24 Lead TSSOP	Tube	-40°C to 85°C
859S0424BGILFT	ICS59S0424BIL	"Lead-Free" 24 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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