Quad-Frequency Programmable VCXO

DATASHEET

General Description

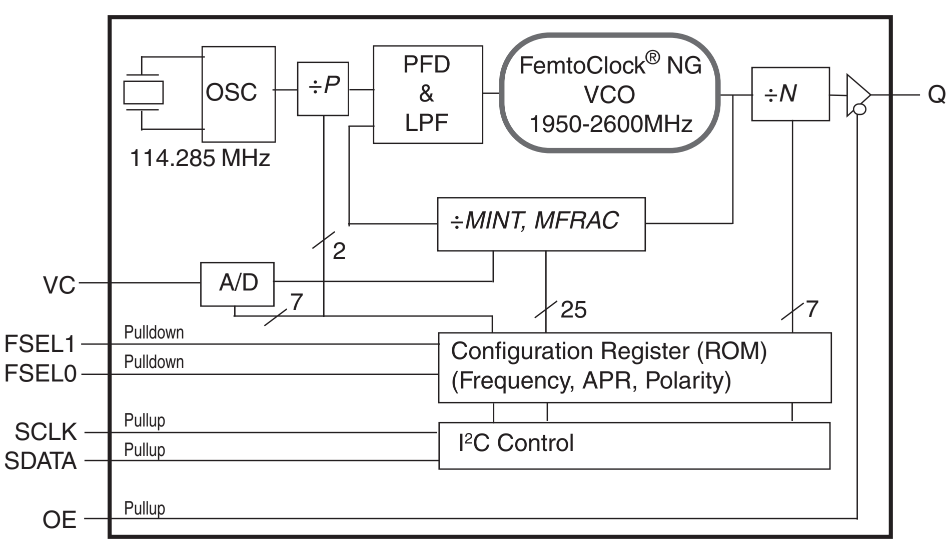
The 8N0QV01 is a Quad-Frequency Programmable VCXO with very flexible frequency and pull-range programming capabilities. The device uses IDT's Fourth Generation FemtoClock® NG technology for an optimum of high clock frequency and low phase noise performance. The device accepts 2.5V or 3.3V supply and is packaged in a small, lead-free (RoHS 6) 10-lead ceramic 5mm x 7mm x 1.55mm package.

Besides the four default power-up frequencies set by the FSEL0 and FSEL1 pins, the 8N0QV01 can be programmed via the I^2C interface to any output clock frequency between 15.476MHz to 260MHz to a very high degree of precision with a frequency step size of 435.9Hz $\div N$ (N: PLL post divider). Since the FSEL0 and FSEL1 pins are mapped to four independent PLL, P, M and N divider registers (P, MINT, MFRAC and N), reprogramming those registers to other frequencies under control of FSEL0 and FSEL1 is supported. The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements.

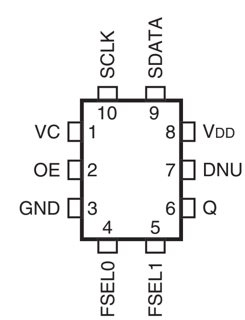
Features

- Fourth generation FemtoClock® NG technology
- Programmable clock output frequency from 15.476MHz to 260MHz
- Four power-up default frequencies (see part number order codes), re-programmable by I^2C
- I^2C programming interface for the output clock frequency, APR and internal PLL control registers
- Frequency programming resolution is 435.9Hz $\div N$
- Absolute pull-range (APR) programmable from ±2.5 to ±727.5ppm
- One 2.5V, 3.3V LVCMOS clock output
- Two control inputs for the power-up default frequency
- LVCMOS/LVTTL compatible control inputs
- RMS phase jitter @ 156.25MHz (12kHz - 20MHz): 0.635ps (typical)
- RMS phase jitter @ 156.25MHz (1kHz - 40MHz): 0.850ps (typical)
- 2.5V or 3.3V supply voltage modes
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

Block Diagram

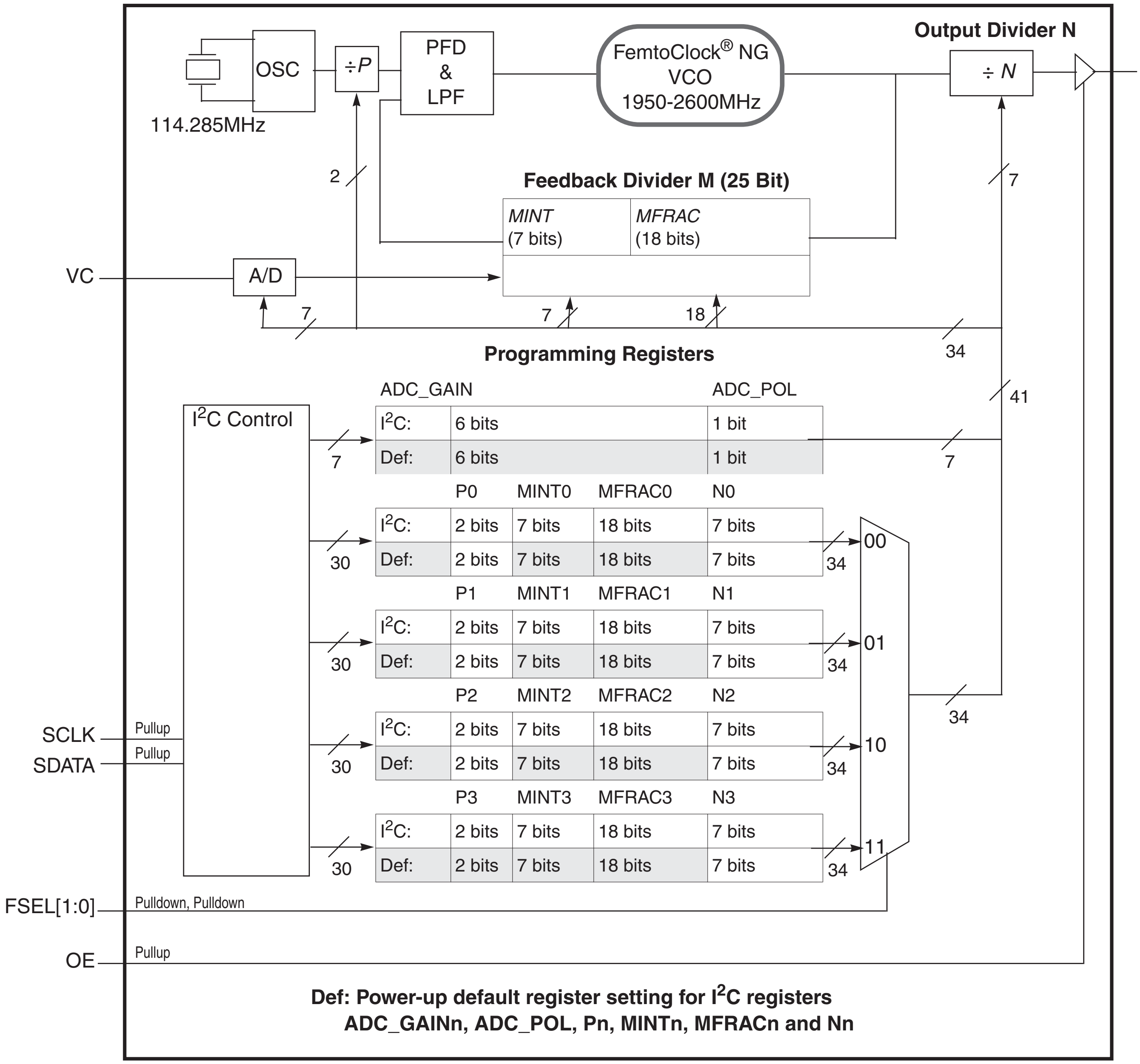


Pin Assignment



IDT8N0QV01 Rev H
10-lead ceramic 5mm x 7mm x 1.55mm package body
CD Package
Top View

Block Diagram with Programming Registers



Pin Description and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1	VC	Input		VCXO Control Voltage. The control voltage versus frequency characteristics are set by the ADC_GAIN[5:0] register bits.
2	OE	Input	Pullup	Output enable pin. See Table 3B for function. LVCMOS/LVTTL interface levels.
3	GND	Power		Power supply ground.
5, 4	FSEL1, FSEL0	Input	Pulldown	Default frequency select pins. LVCMOS/LVTTL interface levels. Refer to the FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information document for default frequency order codes.
6	Q	Output		Clock output. LVCMOS/LVTTL interface levels.
7	DNU			Do not use. Do not connect.
8	V_{DD}	Power		Positive power supply.
9	SDATA	Input	Pullup	I^2C Data Input. LVCMOS/LVTTL interface levels.
10	SCLK	Input	Pullup	I^2C Clock Input. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance		FSEL[1:0], SDATA, SCLK, OE		3.5		pF
			VC		10		pF
C_{PD}	Power Dissipation Capacitance		V_{DD} = 3.465V or 2.625V		8		pF
R_{PULLUP}	Input Pullup Resistor				50		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				50		kΩ
R_{OUT}	Output Impedance	Q	V_{DD} = 3.3V		15		Ω
			V_{DD} = 2.5V		19		Ω

Function Tables

Table 3A. Default Frequency Selection

Input		
FSEL1	FSEL0	Operation
0 (default)	0 (default)	Default frequency 0.
0	1	Default frequency 1.
1	0	Default frequency 2.
1	1	Default frequency 3.

NOTE: The default frequency is the output frequency after power-up. One of four default frequencies is selected by FSEL[1:0]. See programming section for details.

Table 3B. OE Configuration

Input	
OE	Output Enable
0	Output Q are in high-impedance state.
1 (default)	Outputs are enabled.

NOTE: OE is an asynchronous control.

Principles of Operation

The block diagram consists of the internal 3^{rd} overtone crystal and oscillator which provide the reference clock f_{XTAL} of 114.285MHz. The PLL includes the FemtoClock NG VCO along with the pre-divider (*P*), the feedback divider (*M*) and the post divider (*N*). The *P*, *M*, and *N* dividers determine the output frequency based on the f_{XTAL} reference and must be configured correctly for proper operation. The feedback divider is fractional supporting a huge number of output frequencies. The configuration of the feedback divider to integer-only values results in an improved output phase noise characteristics at the expense of the range of output frequencies. In addition, internal registers are used to hold up to four different factory pre-set *P*, *M*, and *N* configuration settings. These default pre-sets are stored in the I^2C registers at power-up. Each configuration is selected via the FSEL[1:0] pins and can be read back using the SCLK and SDATA pins.

The user may choose to operate the device at an output frequency different than that set by the factory. After power-up, the user may write new P, N and M settings into one or more of the four configuration registers and then use the FSEL[1:0] pins to select the newly programmed configuration. Note that the I^2C registers are volatile and a power supply cycle will reload the pre-set factory default conditions.

If the user does choose to write a different *P*, *M*, and *N* configuration, it is recommended to write to a configuration which is not currently selected by FSEL[1:0] and then change to that configuration after the I^2C transaction has completed. Changing the FSEL[1:0] controls results in an immediate change of the output frequency to the selected register values. The *P*, *M*, and *N* frequency configurations support an output frequency range 15.476MHz to 260MHz.

The devices use the fractional feedback divider with a delta-sigma modulator for noise shaping and robust frequency synthesis capability. The relatively high reference frequency minimizes phase noise generated by frequency multiplication and allows more efficient shaping of noise by the delta-sigma modulator.

The output frequency is determined by the 2-bit pre-divider (*P*), the feedback divider (M) and the 7-bit post divider (*N*). The feedback divider (*M*) consists of both a 7-bit integer portion (*MINT*) and an 18-bit fractional portion (*MFRAC*) and provides the means for high-resolution frequency generation. The output frequency f_{OUT} is calculated by:

$$f_{OUT} = f_{XTAL} \cdot \frac{1}{P \cdot N} \cdot \left[MINT + \frac{MFRAC + 0.5}{2^{18}} \right] \quad (1)$$

The four configuration registers for the *P, M (MINT & MFRAC)* and *N* dividers which are named Pn, MINTn, MFRACn and Nn with n = 0 to 3. “n” denominates one of the four possible configurations.

As identified previously, the configurations of *P, M (MINT & MFRAC)* and *N* divider settings are stored the I^2C register, and the configuration loaded at power-up is determined by the FSEL[1:0] pins.

Table 4. Frequency Selection

Input		Selects	Register
FSEL1	FSEL0		
0 (def.)	0 (def.)	Frequency 0	P0, MINT0, MFRAC0, N0
0	1	Frequency 1	P1, MINT1, MFRAC1, N1
1	0	Frequency 2	P2, MINT2, MFRAC2, N2
1	1	Frequency 3	P3, MINT3, MFRAC3, N3

Frequency Configuration

An order code is assigned to each frequency and VCXO pull range configuration programmed by the factory (default frequencies). For available order codes, see the *FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information* document.

For more information and guidelines on programming of the device for custom frequency configurations, programming for a specific VCXO pull range, the available APR (absolute pull range), the register description and the serial interface description, see the *FemtoClock NG Ceramic 5x7 Module Programming Guide.*

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	3.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVCMOS)	-0.5V to V_{DD} + 0.5V
Outputs, I_O (SDATA)	10mA
Package Thermal Impedance, θ_{JA}	49.4°C/W (mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 5A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current	No Load, OE = Low		135	150	mA

Table 5B. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current	No Load, OE = Low		130	145	mA

Table 5C. LVCMOS/LVTTL DC Characteristic, V_{DD} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	OE, SCLK, SDATA, FSEL[1:0]	V_{DD} = 3.3V	2		V_{DD}+ 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	OE, SCLK, SDATA, FSEL[1:0]	V_{DD} = 3.465V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	OE,	V_{DD} = V_{IN} = 3.465V or 2.625V			10	µA
		SDATA, SCLK	V_{DD} = V_{IN} = 3.465V or 2.625V			5	µA
		FSEL0, FSEL1	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	OE	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-500			µA
		SDATA, SCLK	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
		FSEL0, FSEL1	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage	Q	V_{DD} = 3.465V	2.4			V
			V_{DD} = 2.625	1.7			V
V_{OL}	Output Low Voltage	Q	V_{DD} = 3.6V or 2.625			0.4	V

AC Electrical Characteristics

Table 6A. AC Characteristics, V_{DD} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Q, nQ	*P* = 1, *N* = 10...126	15.476		260	MHz
f_I	Initial Accuracy	Measured at 25°C at Final Test			±10	ppm
fS	Temperature Stability	Option code = A or B			±100	ppm
		Option code = E or F			±50	ppm
		Option code = K or L			±20	ppm
f_A	Aging	Frequency drift over 10 year life			±3	ppm
		Frequency drift over 15 year life			±5	ppm
f_T	Total Stability	Option code A or B (10 year life)			±113	ppm
		Option code E or F (10 year life)			±63	ppm
		Option code K or L (10 year life)			±33	ppm
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1	V_{DD} = 3.3V		15	32	ps
		V_{DD} = 2.5V		18	40	ps
*t*jit(per)	Period Jitter; NOTE 1	V_{DD} = 3.3V		2.6	5	ps
		V_{DD} = 2.5V		4	7	ps
*t*jit(Ø)	RMS Phase Jitter (Random)	17MHz ≤ f_{out} ≤ 260MHz, Integration Range: 12kHz - 20MHz, NOTE 3		0.70	1.20	ps
		156.25MHz, Integration Range: 12kHz - 20MHz; NOTE 2		0.64	0.92	ps
		156.25MHz, Integration Range: 1kHz - 40MHz		0.85	1.00	ps
Φ_N(100)	Single-side band phase noise, 100Hz from Carrier	156.25MHz		-75		dBc/Hz
Φ_N(1k)	Single-side band phase noise, 1kHz from Carrier	156.25MHz		-98		dBc/Hz
Φ_N(10k)	Single-side band phase noise, 10kHz from Carrier	156.25MHz		-118		dBc/Hz
Φ_N(100k)	Single-side band phase noise, 100kHz from Carrier	156.25MHz		-127		dBc/Hz
Φ_N(1M)	Single-side band phase noise, 1MHz from Carrier	156.25MHz		-139		dBc/Hz
Φ_N(10M)	Single-side band phase noise, 10MHz from Carrier	156.25MHz		-143		dBc/Hz
t_R / t_F	Output Rise/Fall Time	V_{DD} = 3.3V, 20% to 80%	150	425	700	ps
		V_{DD} = 2.5V, 20% to 80%	150	500	800	ps
odc	Output Duty Cycle		45	50	55	%
t_{OSC}	Oscillator Start-Up Time				20	ms
t_{SET}	Output frequency settling time after FSEL0 and FSEL1 values are changed				1	ms

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All AC parameters are characterized with P = 1.
NOTES continued on next page.

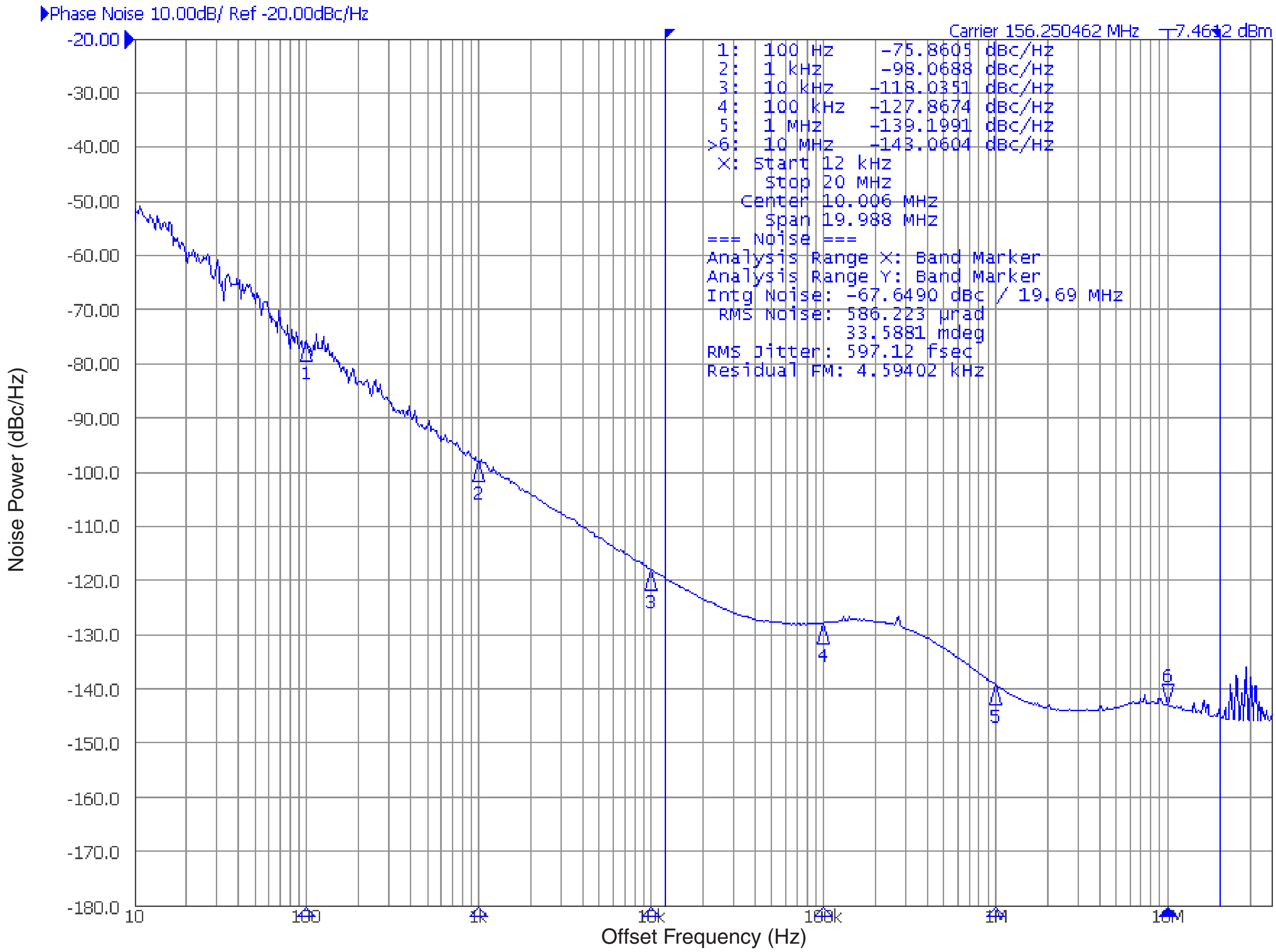
NOTE: Please see the FemtoClock Ceramic 5x7 Modules Programming Guide for more information on PLL feedback modes and the optimum configuration for phase noise.
NOTE 1: This parameter is defined in accordance with JEDEC standard 65.
NOTE 2: Please refer to the phase noise plots.
NOTE 3: Applies to output frequencies: 17MHz, 19.44MHz, 25MHz, 33.33MHz, 75MHz, 77.76MHz, 100MHz, 106.25MHz, 122.88MHz, 125MHz, 150MHz, 155.52MHz, 156.25MHz, 161.132MHz, 175MHz, 187.5MHz, 200MHz, 212.5MHz, 250MHz and 260MHz.

Table 6B. VCXO Control Voltage Input (V_C) Characterisitics,

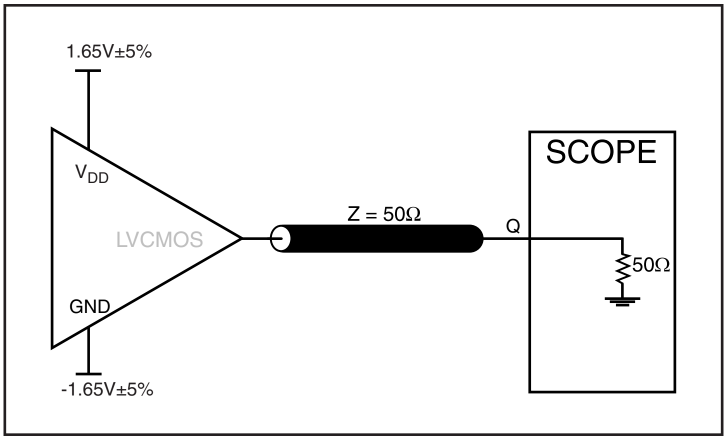
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
K_V	Oscillator Gain, NOTE 1, 2, 3	V_{DD} = 3.3V	7.57		477.27	ppm/V
		V_{DD} = 2.5V	10		630	ppm/V
L_{VC}	Control Voltage Linearity; NOTE 4	BSL Variation	-5	±0.4	+5	%
BW	Modulation Bandwidth			100		kHz
Z_{VC}	VC Input Impedance			500		kΩ
VC_{NOM}	Nominal Control Voltage			$V_{DD}/2$		V
V_C	Control Voltage Tuning Range; NOTE 4	V_{DD} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C	0		V_{DD}	V

NOTE 1: V_C = 0V to V_{DD}. Oscillator gain is programmed by IDT. Gain = (25 · n) ÷ V_{CC} and is in the range of n=1 to n = 63.
NOTE 2: Nominal oscillator gain: Please refer to the FemtoClock NG Ceramic 5x7 Module Programming Guide document.
NOTE 3: For best phase noise performance, use the lowest K_V that meets the requirements of the application.
NOTE 4: BSL = Best Straight Line Fit: Variation of the output frequency vs. control voltage V_C, in percent. V_C ranges from 10% to 90% V_{DD}.

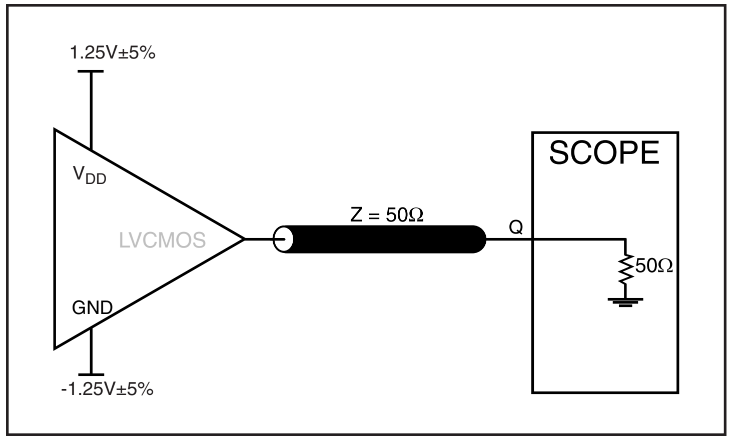
Typical Phase Noise at 156.25MHz (12kHz - 20MHz)



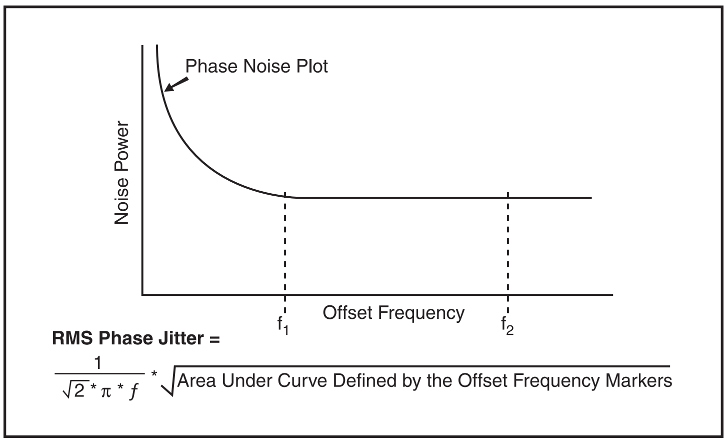
Parameter Measurement Information



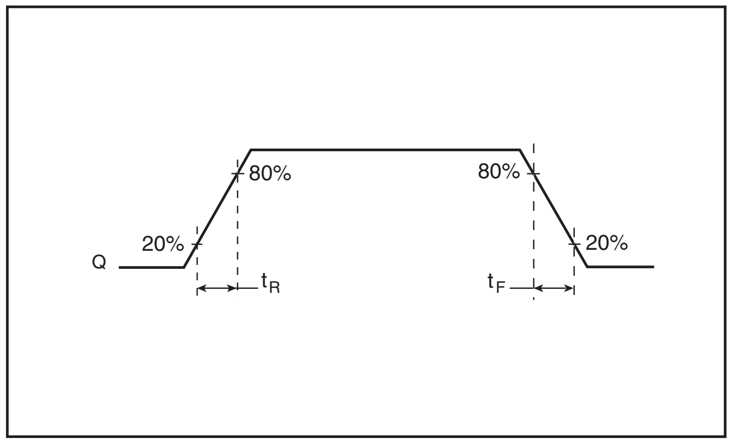
3.3V LVCMOS Output Load Test Circuit



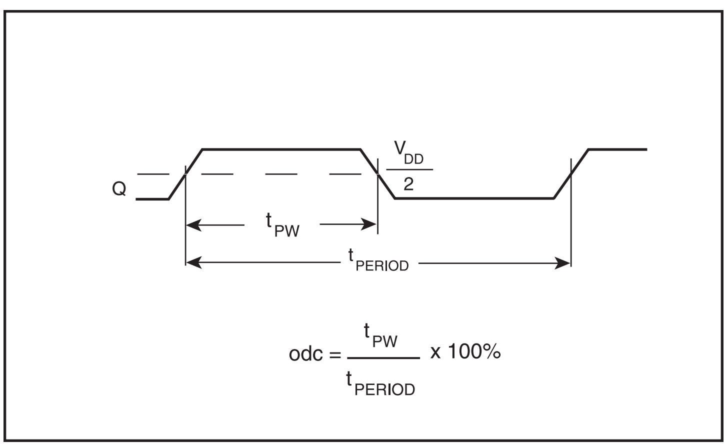
2.5V LVCMOS Output Load Test Circuit



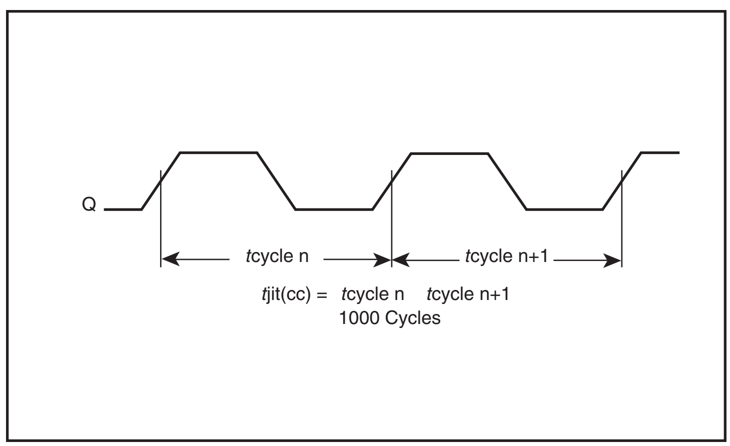
RMS Phase Jitter



Output Rise/Fall Time

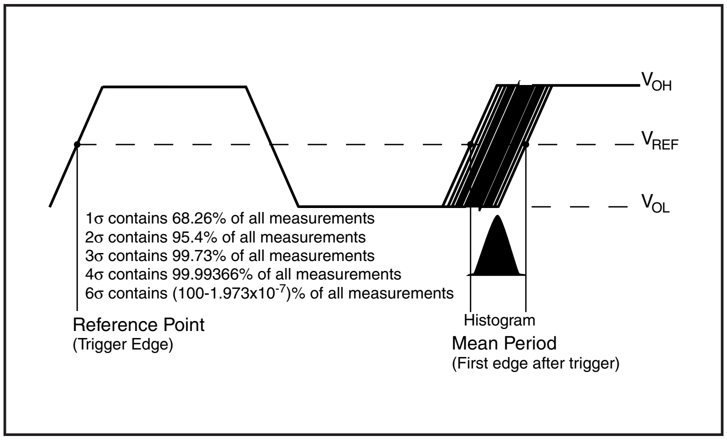


Output Duty Cycle/Pulse Width/Period



Cycle-to-Cycle Jitter

Parameter Measurement Information, continued



Period Jitter

Applications Information

Recommendations for Unused Input Pins

Inputs:

LVCMOS Select Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Schematic Example

Figure 1 shows an example 8N0QV01application schematic in which the device is operated at V_{DD} = +3.3V. The schematic example focuses on functional connections and is intended as an example only and may not represent the exact user configuration. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set. For example OE and FSEL[1:0] can be configured from an FPGA instead of set with pull up and pull down resistors as shown.

The 8N0QV01 is not a self contained part; it requires pairing with a PLL. The two connections necessary to be made to the PLL are VC, the analog control voltage that sets the center frequency of the VCXO, and Q, which is the oscillator output. VC is the analog output of the PLL low pass loop filter that serves to remove noise from the phase detector error output.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise, so to achieve optimum jitter performance isolation of the V_{DD} pin from the power supply is required. In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µF capacitor on the V_{DD} pin must be placed on the device side with direct return to the ground plane though vias. The remaining filter components can be on the opposite side of the PCB.

Power supply filter component recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

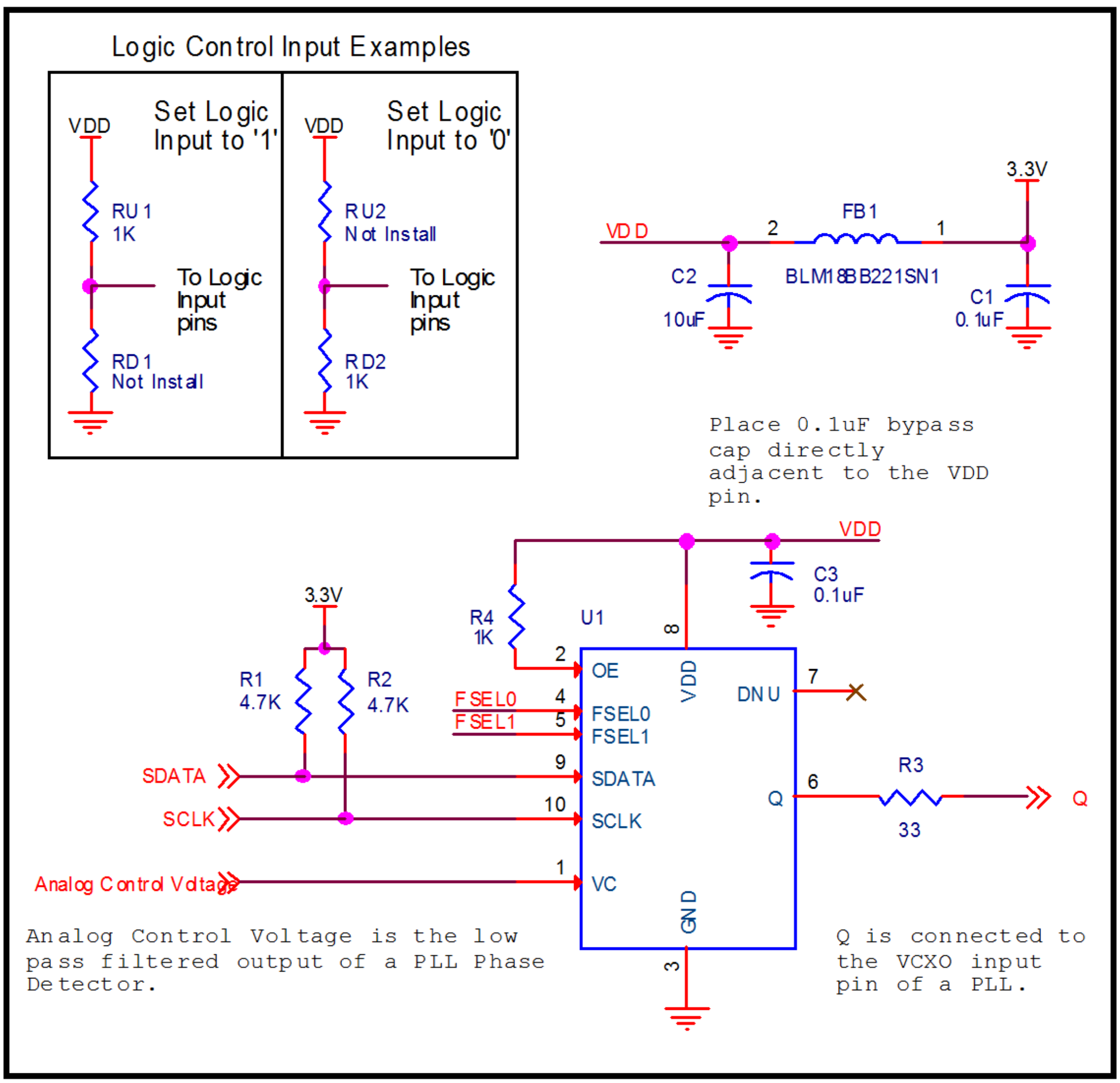


Figure 1. IDT8N0QV01 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8N0QV01.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8N0QV01 is the sum of the core power plus the power dissipation in the load(s). The following is the power dissipation for V_{DD} = 3.3V +5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD}$ = 3.465V * 150mA = **519.8mW**

Total Static Power:

= Power $(core)_{MAX}$ = **519.8mW**

Dynamic Power Dissipation at F_{OUT} (max)

Total Power (F_{OUT_MAX}) = [(C_{PD} * N) * Frequency * $(V_{DD})^2$**]** = [(8pF *1) * 260MHz * $(3.465V)^2$] = **24.97mW**

Total Power

= Static Power + Dynamic Power Dissipation
= 519.8mW + 24.97mW
= 544.77mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 49.4°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.545W *49.4°C/W = 112°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for a 10-lead Ceramic 5mm x 7mm Package, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	49.4°C/W	44.2°C/W	41.0°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 10-lead Ceramic 5mm x 7mm Package

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	49.4°C/W	44.2°C/W	41.0°C/W

Transistor Count

The transistor count for IDT8N0QV01 is: 47,302

Package Outline and Package Dimensions

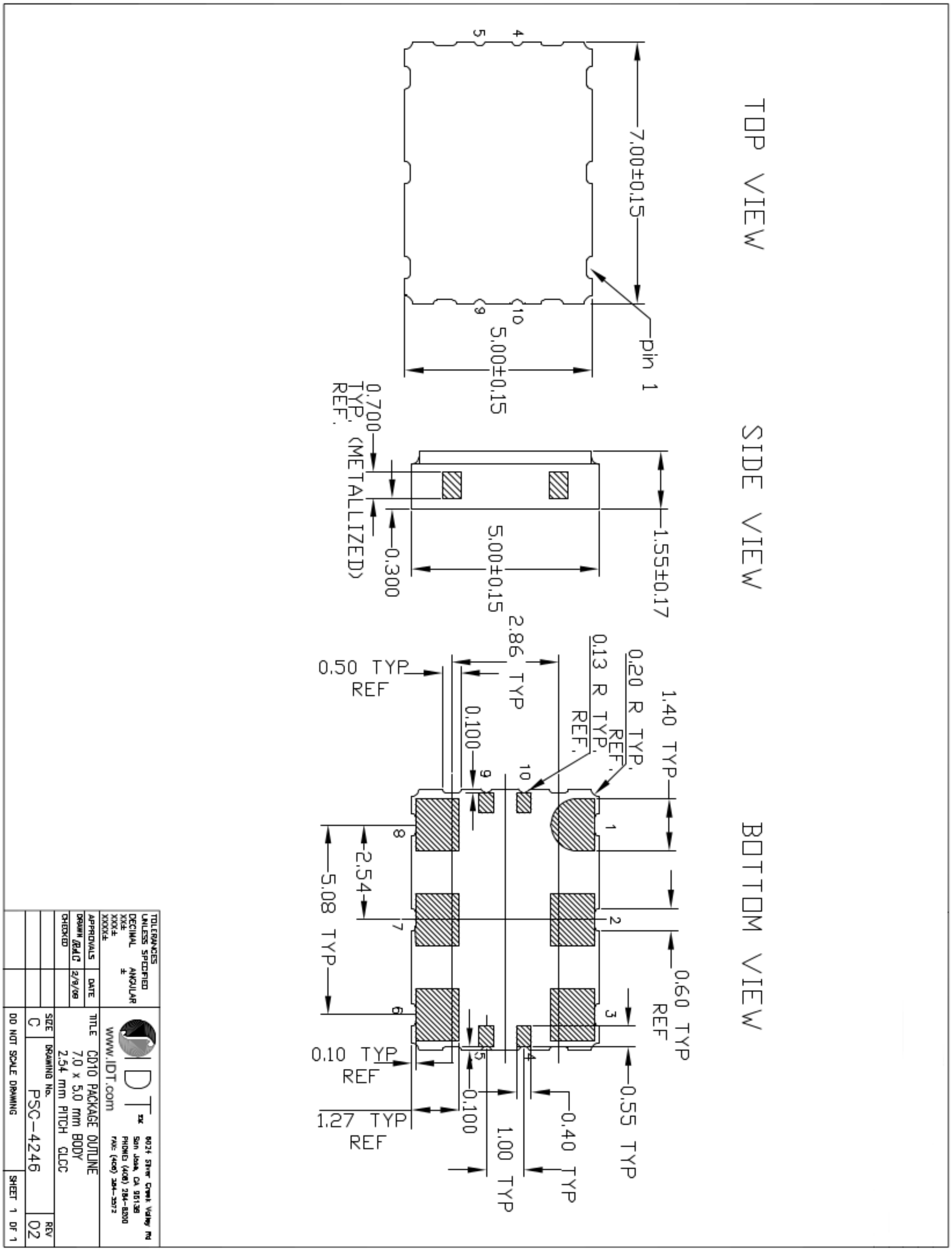


Table 9. Device Marking

Marking	Industrial Temperature Range (T_A = -40°C to 85°C)	Commercial Temperature Range (T_A = 0°C to 70°C)
	IDT8N0QV01**y**H-**dddd**CDI	IDT8N0QV01**y**H-**dddd**CD
	y = Option Code, **dddd**=Default-Frequency and VCXO Pull Range	

NOTE: For available order codes, see the FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information document.

For more information and guidelines on programming of the device for custom frequency configurations, programming for a specific VCXO pull range, the available APR (absolute pull range), the register description and the serial interface description, see the FemtoClock NG Ceramic 5x7 Module Programming Guide.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T1 6A 6B 	3 8 9 14	first row: deleted '(see Table 3C).' forth row: replaced description. Deleted NOTE 2 from RMS Phase Jitter. Added 'NOTE 2' to 156.25MHz. Note 2: Added 'Please refer to the FemtoClock NG Ceramic 5x7 Module Programming Guide document.' Power Considerations. Changed Dynamic Power Dissipation from 2.5mW to 24.97mW	3/14/2014

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