Register Descriptions

The register descriptions section describes the behavior and function of the customer-programmable non-volatile-memory registers in the 9FGV1006 clock generator.

For details of product operation, refer to the product datasheet.

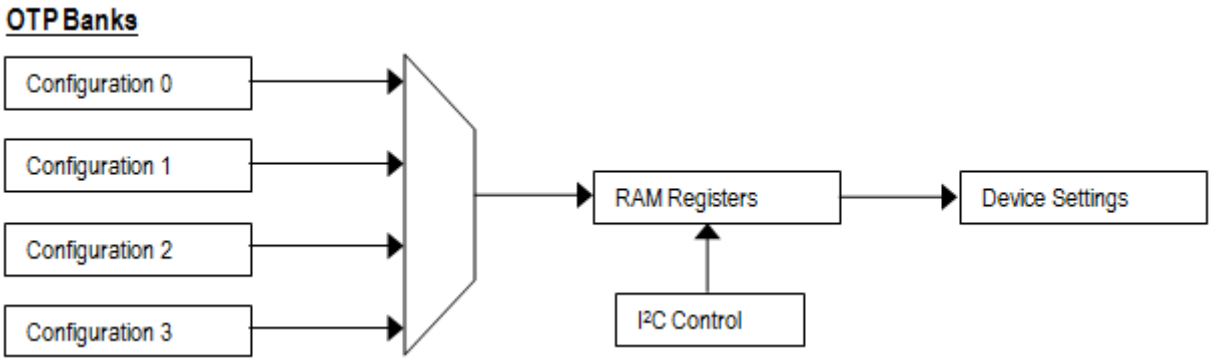
9FGV1006 Clock Register Set

The device contains volatile (RAM) 8-bit registers and non-volatile 8-bit registers (Figure 1). The non-volatile registers are One-Time Programmable (OTP) and will be pre-programmed at the factory with a custom dash-code configuration.

The device operates according to settings in the RAM registers. At power-up a pre-programmed configuration is transferred from OTP to RAM registers. The device behavior can then be modified by reprogramming the RAM registers through I^2C.

The device can start up in "I^2C mode" or in "Hardware Select Mode", depending upon the status of the REF0_SEL_I2C# pin at power up. Also see the datasheet. I^2C access is only possible when the device has started up in I^2C mode. Startup in I^2C mode is default when no pull-up is added to the REF0_SEL_I2C# pin. Pre-programming settings determine which of the 4 OTP banks is loaded into RAM registers at power up in I^2C mode. Using I2C commands the configuration can be changed and there are also commands to reload a configuration from a different OTP bank.

Figure 1. Register Maps



User Configuration Selection

At power-up, the voltage at REF0_SEL_I2CB pin 23 is latched by the part and used to select the state of SEL0/SCL and SEL1/SDA pins (Table 1).

When a weak pull-up (10kΩ) is placed on REF0_SEL_I2C#, the SEL0/SCL and SEL1/SDA pins will be configured as hardware select inputs, SEL0 and SEL1. Connecting SEL0 and SEL1 to VDDD and/or GND selects one of 4 configuration register sets, CFG0 through CFG3, which is then loaded into the non-volatile configuration registers to configure the clock synthesizer. The CFG0 through CFG3 configurations are preprogrammed at the factory according to customer specifications and assigned a specific (dash) part number.

When a weak pull-down is placed on REF0_SEL_I2C# (or when it is left floating to use internal pull-down), the pins SEL0 and SEL1 will be configured as an I^2C interface's SDA and SCL slave bus. Configuration register set CFG0 is commonly loaded into the non-volatile configuration registers to configure the clock synthesizer but the device can be configured to load any of the other configurations. The host system can use the I^2C bus to update the volatile RAM registers to change the configuration, and to read status registers.

Table 1. Power-Up Setting of Hardware Select Pin vs I²C Mode, and Default OTP Configuration Register

REF0_SEL_I2CB Strap at Power-Up	SEL1/SDA pin	SEL0/SCL pin	Function
10kΩ pull-up	0	0	OTP bank CFG0 used to initialize RAM configuration registers.
	0	1	OTP bank CFG1 used to initialize RAM configuration registers.
	1	0	OTP bank CFG2 used to initialize RAM configuration registers.
	1	1	OTP bank CFG3 used to initialize RAM configuration registers.
10kΩ pull-down or floating	SDA	SCL	I²C bus enabled to access registers. OTP bank CFG0 used to initialize RAM configuration registers.

I²C Interface and Register Access

When powered up in I²C mode, the device allows access to internal RAM registers. The default device address is 0xD0 for 8 bits or 0x68 for 7 bits. The device can be preprogrammed for addresses in the range 0xD0-D2-D4-D6 for 8 bits or 0x68-69-6A-6B for 7 bits. The device acts as a slave device on the I²C bus using one of the four I²C addresses to allow multiple devices to be used in the system. The interface accepts byte-oriented block write and block read operations. Two address bytes specify the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP signal is received, at which point, all data received in the block write will be written simultaneously in the registers.

For full electrical I²C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 100kΩ typical.

Figure 2. I²C R/W Sequence

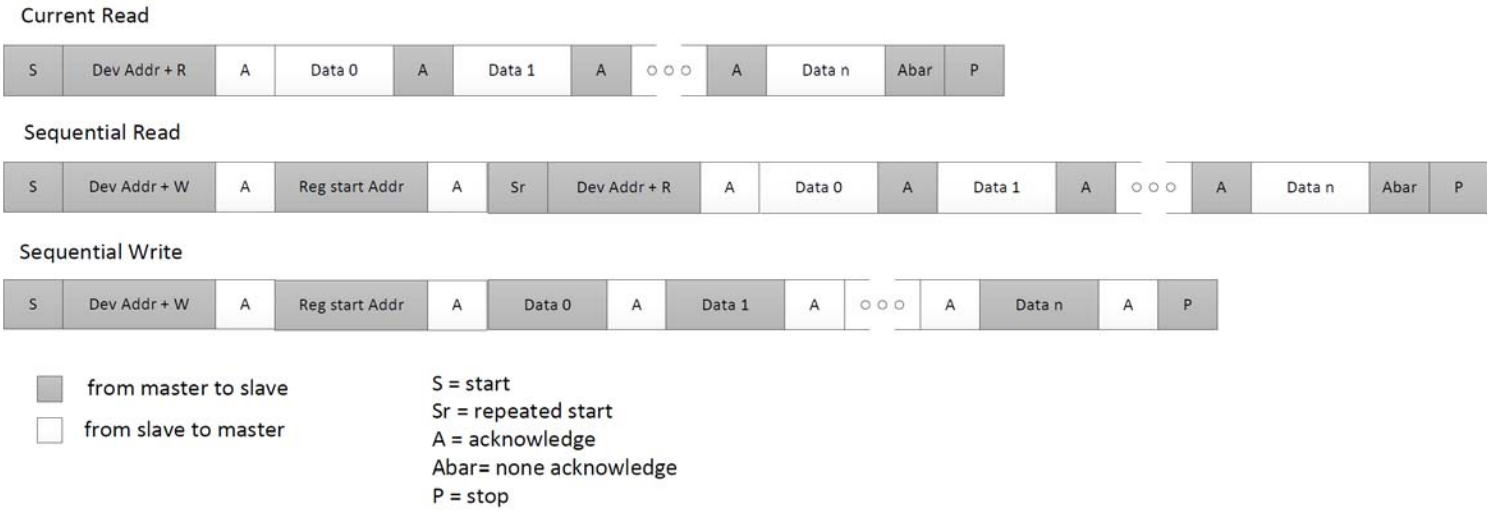


Table 2. RAM Overview

Register Address	Function Description
0x00	Device / I^2C settings.
0x01	REF output settings.
0x02	Reserved.
0x03	
0x04	
0x05	OUT1 output settings.
0x06	
0x07	
0x08	Reserved.
0x09	
0x0A	
0x0B	OUT0 output settings.
0x0C	
0x0D	
0x0E	Crystal oscillator settings.
0x0F	
0x10	Fractional feedback divider (FFD) spread spectrum settings.
0x11	
0x12	FFD integer value.
0x13	FFD fractional value.
0x14	
0x15	FFD spread spectrum settings.
0x16	
0x17	FFD miscellaneous.
0x18	
0x19	
0x1A	PLL miscellaneous.
0x1B	
0x1C	PLL loop filter settings.
0x1D	
0x1E	
0x1F	PLL feedback divider value.

Table 2. RAM Overview

Register Address	Function Description
0x20	Integer output divider values.
0x21	
0x22	
0x23	Reserved.
0x24	Reserved.
0x25	Miscellaneous device settings.

See Table 3 for details at the bit level.

Table 3. RAM Register Map

Register Address		Register Bit	Default	Function Description
Decimal	Hex			
00	0x00	7	0	Device preprogrammed? 0 = no, 1 = yes.
		[6..5]	00	I^2C device address. 00 = 0xD0 / 0x68, 01 = 0xD2 / 0x69, 10 = 0xD4 / 0x6A, 11= 0xD6 / 0x6B [1].
		[4..2]	00	Reserved.
		[1..0]	00	Load configuration number at power-up [2].
01	0x01	[7..6]	11	Enable REF outputs: 0x = REF0 disabled (unused), 1x = REF0 enabled.
		5	0	Reserved.
		4	0	Behavior when REF is unused: 0 = Logic “0”, 1 = High impedance (tri-state).
		[3..2]	11	REF outputs power supply voltage: 00 = 01 = 1.8V, 10 = 2.5V, 11 = 3.3V.
		[1..0]	11	Reserved.
02	0x02	[7..0]	8F-hex	Reserved.
03	0x03	[7..0]	01-hex	Reserved.
04	0x04	[7..0]	44-hex	Reserved.
05	0x05	7	1	Enable OUT1: 0 = disabled (unused), 1 = enabled.
		[6..4]	000	OUT1 configuration: 000 = LP-HCSL, Low-power HCSL. 001 = CMOS1, Single-ended CMOS on true output pin. 011 = LVDS. 100 = CMOS2, Single-ended CMOS on complementary output pin. 101 = CMOSD, Differential CMOS. 111 = CMOSP, Two single-ended CMOS outputs, in-phase. 010 and 110 are not used.
		[3..2]	11	OUT1 power supply voltage: 00 = 01 = 1.8V, 10 = 2.5V, 11 = 3.3V.
		[1..0]	11	Reserved.

Table 3. RAM Register Map (Cont.)

Register Address		Register Bit	Default	Function Description
Decimal	Hex			
06	0x06	7	0	Reserved.
		6	0	Behavior when OUT1 is unused: 0 = Logic “0”, 1 = High impedance (tri-state).
		5	1	OUT1 LP-HCSL slew rate control: 0 = slow, 1 = fast.
		4	1	OUT1 LP-HCSL impedance control: 0 = 85Ω differential, 1 = 100Ω differential.
		[3..0]	0001	OUT1 LP-HCSL amplitude control: 650mVpp at 0000–950mVpp at 1111.
07	0x07	7	0	Reserved.
		[6..4]	101	OUT1 LVDS common mode control: 8µA at 000–11.5µA at 111.
		3	0	Reserved.
		[2..0]	100	OUT1 LVDS amplitude control: 30µA at 000–65µA at 111.
08	0x08	[7..0]	8F-hex	Reserved.
09	0x09	[7..0]	01-hex	Reserved.
10	0x0A	[7..0]	44-hex	Reserved.
11	0x0B	7	1	Enable OUT0: 0 = disabled (unused), 1 = enabled.
		[6..4]	000	OUT0 configuration: 000 = LP-HCSL, Low-power HCSL. 001 = CMOS1, Single-ended CMOS on true output pin. 011 = LVDS. 100 = CMOS2, Single-ended CMOS on complementary output pin. 101 = CMOSD, Differential CMOS. 111 = CMOSP, Two single-ended CMOS outputs, in-phase. 010 and 110 are not used.
		[3..2]	11	OUT0 power supply voltage: 00 = 01 = 1.8V, 10 = 2.5V, 11 = 3.3V.
		[1..0]	11	Reserved.
12	0x0C	7	0	Reserved.
		6	0	Behavior when OUT0 is unused: 0 = Logic “0”, 1 = High impedance (tri-state).
		5	0	OUT0 LP-HCSL slew rate control: 0 = slow, 1 = fast.
		4	0	OUT0 LP-HCSL impedance control: 0 = 85Ω differential, 1 = 100Ω differential.
		[3..0]	0001	OUT0 LP-HCSL amplitude control: 650mVpp at 0000–950mVpp at 1111.
13	0x0D	7	0	Reserved.
		[6..4]	100	OUT0 LVDS common mode control: 8µA at 000–11.5µA at 111.
		3	0	Reserved.
		[2..0]	100	OUT0 LVDS amplitude control: 30µA at 000–65µA at 111.

Table 3. RAM Register Map (Cont.)

Register Address		Register Bit	Default	Function Description
Decimal	Hex			
14	0x0E	7	1	Crystal oscillator LDO: 0 = disabled, 1 = enabled.
		6	0	Reserved.
		[5..0]	000101	Crystal oscillator X1 pin capacitance: Cap (pF) = 10 + 0.44 × Bits[4..0] + 7.04 × Bit[5]. See section Crystal Load Capacitance Registers for crystal oscillator load capacitance configuration.
15	0x0F	7	1	Crystal oscillator circuit: 0 = Disabled, 1 = Enabled.
		6	0	Reserved.
		[5..0]	000101	Crystal oscillator X2 pin capacitance: Cap (pF) = 7.98 + 0.442 × Bits[4..0] + 7.072 × Bit[5].
16	0x10	7	0	Fractional feedback divider (FFD) spread spectrum: 0 = disabled, 1 = enabled.
		[6..4]	000	Reserved.
		[3..0]	0000	FFD spread spectrum period, bits[11..8]. See section Fractional Feedback Divider and Spread Spectrum for spread spectrum configuration.
17	0x11	[7..0]	00-hex	FFD spread spectrum period, bits[7..0].
18	0x12	[7..0]	0C-hex	FFD integer value. See section Fractional Output Divider Configuration for fractional feedback divider configuration.
19	0x13	[7..0]	80-hex	FFD fractional value, bits[15..8].
20	0x14	[7..0]	00-hex	FFD fractional value, bits[7..0].
21	0x15	[7..0]	00-hex	FFD spread spectrum step, bits[15..8].
22	0x16	[7..0]	00-hex	FFD spread spectrum step, bits[7..0].
23	0x17	[7..0]	00-hex	Reserved.
24	0x18	7	1	FFD reset-B: 0 = hold FFD in reset mode, 1 = release FFD. Toggle to 0 and back to 1 to apply a reset or restart of the FFD.
		[6..2]	00000	Reserved.
		1	0	FFD integer mode: 0 = use fractional settings for a fractional feedback divider value. 1 = run feedback divider in integer mode in case the value is an integer (for best performance).
		0	1	Enable FFD: 0 = FFD is disabled, 1 = FFD is enabled.
25	0x19	[7..0]	00-hex	Reserved.

Table 3. RAM Register Map (Cont.)

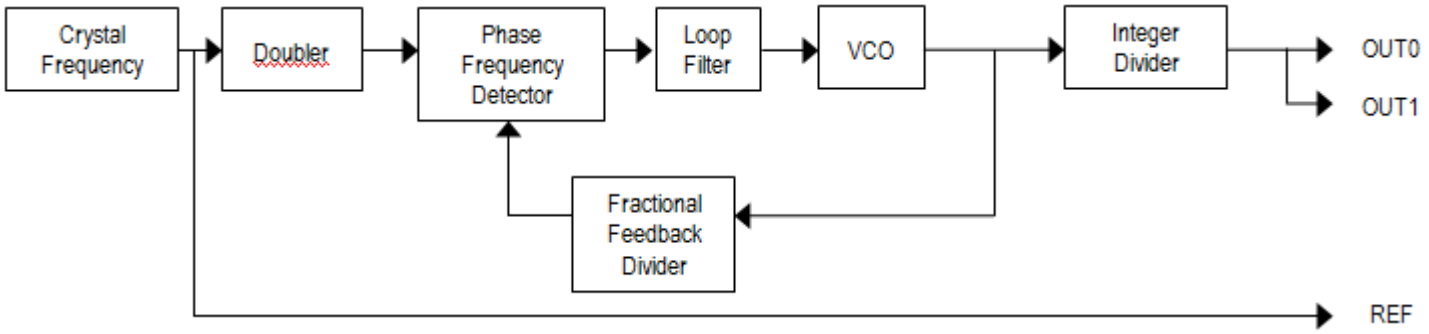
Register Address		Register Bit	Default	Function Description
Decimal	Hex			
26	0x1A	7	1	PLL, VCO band calibration start. Toggle to 0 and back to 1 to trigger a calibration. The calibration engages at the moment the bit moves from 0 to 1. The calibration finds the optimum VCO band for the current VCO frequency.
		6	0	Override VCO band: 0 = use calibrated VCO band, 1 = use VCO band value in bits [5..0].
		[5..0]	100000	VCO band value. See bit 6.
27	0x1B	7	1	Enable VCO: 0 = VCO disabled, 1 = VCO enabled.
		6	1	Enable charge pump: 0 = CP disabled, 1 = CP enabled.
		5	1	Enable PLL bias: 0 = PLL bias disabled, 1 = PLL bias enabled.
		4	1	Bypass 3rd pole in loop filter: 0 = use 3rd pole, 1 = 3rd pole bypassed.
		[3..0]	1100	Reserved.
28	0x1C	[7..4]	1010	Loop filter R-zero value.
		[3..0]	1111	Reserved.
29	0x1D	[7..0]	00-hex	Reserved.
30	0x1E	[7..4]	0000	Reserved.
		[3..0]	1010	Charge pump current, 0 to 750µA with step of 50µA.
31	0x1F	[7..0]	32-hex	Reserved.
32	0x20	[7..0]	19-hex	Reserved.
33	0x21	[7..0]	19-hex	Integer output divider value, bits [7..0].
34	0x22	[7..4]	0000	Integer output divider value, bits [11..8].
		[3..0]	0000	Reserved.
35	0x23	[7..0]	00-hex	Reserved.
36	0x24	[7..0]	F1-hex	Reserved.
37	0x25	7	0	Reserved.
		6	1	Enable Integer output divide: 0 = disabled, 1 = enabled.
		5	1	Enable crystal frequency doubler: 0 = disabled, 1 = enabled.
		[4..3]	01	Reserved.
		2	1	Integer output divide enable: 0 = disabled, 1 = enabled.
		[1..0]	01	Reserved.

[1] To be able to read this info you already need to know the device address.

[2] These two bits show the configuration number 0~3 that will be loaded from OTP into registers at power up. When changing these bits through I^2C you instruct the chip to load another configuration from OTP. This is useful for switching between OTP configurations when in I^2C mode. This method is also used to step through each configuration for reading back OTP contents.

Block Diagram

Figure 3. 9FGV1006 Block Diagram



Equations:

FVCO = FCRYSTAL × Doubler × (Fractional Feedback Divider × 2)(see registers 0x10–0x19).
FOUT0 = FOUT1 = FVCO / Integer Divider (see registers 0x21 and 0x22).
Doubler is ×2 when enabled and ×1 when disabled.
The total feedback divider value is the fractional counter settings with an additional ×2.

Limits:

FCRYSTAL: 10MHz–40MHz
FVCO: 2300MHz–2600MHz
Integer Output Divider: 8–4095
Feedback Divider: 12–255

Fractional Output Divider Configuration

The Fractional feedback divider (FFD) is composed of an 8-bit integer portion (address 0x12) and a 16-bit fractional portion (addresses 0x13 and 0x14).

FFD value P = INT(P) + FRAC(P) = FVCO / FPFD (1)
FFD Integer [7..0] = DEC2HEX(INT(P)) (2)

The FFD divides the VCO frequency FVCO down to the phase-frequency detector frequency FPFD. Note the additional divide by 2, so $F_{PFD} = F_{VCO} / (2 \times P)$.

Convert FRAC(P) to hex with Eq.2 where ROUND2INT means to round to the nearest integer. The round-off error of P in ppm is the output frequency error in ppm.

FFD fraction [15..0] = DEC2HEX(ROUND2INT(216×FRAC(P))) (3)

Example: Assume a 25MHz crystal, 122.88MHz output clocks and the VCO frequency is 20 × 122.88MHz = 2457.6MHz.

The phase frequency detector frequency F_{PFD} = 2 × 25MHz = 50MHz and the FFD value is 2457.6 / 2 / 50 = 24.576.

The integer portion is 24, so address 0x12 will be 18-hex. The fractional portion is 0.576.

FFD Fraction [15..0] = DEC2HEX(ROUND2INT(216×0.576) = DEC2HEX(ROUND2INT(37748.736)) = DEC2HEX(37749) = 93 75.

Address 0x13 = 93-hex and address 0x14 = 75-hex.

There is a small error from the rounding. The actual FFD value is 24 + 37749 / 216 = 24.576004028. The rounding error is 24.576004028 / 24.576 - 1 = 0.16ppm.

Fractional Feedback Divider and Spread Spectrum

Spread spectrum capability is contained within the Fractional-N feedback divider associated with the PLL. When applied, triangle wave modulation of any spread spectrum amount, SS%AMT up to ±2.5% center spread and -5% down spread between 30 and 63kHz may be generated, independent of the output clock frequency. Five variables define spread spectrum in the FFD (see Table 4).

Table 4. Spread Spectrum Variables in the FFD

Name	Function	RAM Register	Note
SS Enable	Spread spectrum control enable	0x10 [7].	When SS Enable = 0, contents of Period and Step registers are Don't Care. When SS Enable = 1, enables the spread spectrum modulation.
FOD Integer	Integer portion of the FOD value P	0x12 [7..0].	See equations 4 and 5 below.
FOD Fraction	Fractional portion of the FOD value P	0x13 [7..0] = Fraction [15..8]. 0x14 [7..0] = Fraction [7..0].	See equations 4 and 5 below.
SS Period	Spread spectrum modulation period	0x10 [3..0] = Period [11..8]. 0x11 [7..0] = Period [7..0].	Total 12-bits for the period. Defined as half the reciprocal of the modulation frequency and measured in cycles of the FFD output frequency. See equation 6 below.
SS Step	Modulation step size	0x15 [7..0] = Step [15..8]. 0x16 [7..0] = Step [7..0].	Sets the time rate of change or time slope of the output clock frequency. See equation. 8 below.

Equations:

To calculate the spread spectrum registers, first determine the value in decimal of the FFD output divider P. The value of P will be the top of the triangle modulation wave. In case of Down Spread, this is perfect so we can use P as is. In case of Center Spread, we need to offset P.

Down spread:

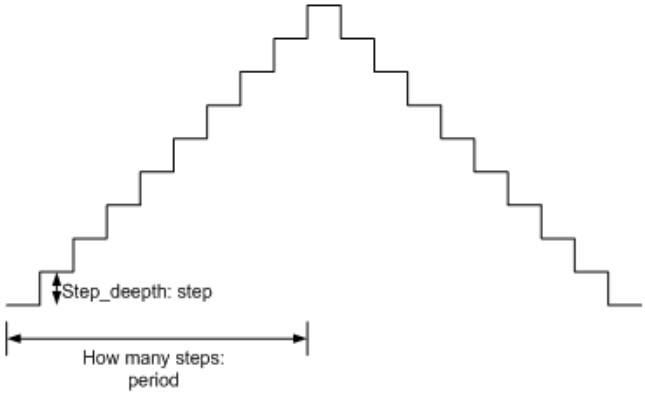
- FFD value P = INT(P) + FRAC(P) = FVCO / (2 × FPFD) (4)
- See equations 2 and 3 in section Fractional Output Divider Configuration for address 0x12, 0x13 and 0x14 settings.

Center spread:

- FFD value P = INT(P) + FRAC(P) = (1 - SS% / 200) × (FVCO / (2 × FPFD)) (5)
- Note that the SS% value is the peak-to-peak value. so with ±1.0% center spread, the SS% value is 2.0%

Consider one cycle of down spread triangular modulation; the FFD value is ramped down linearly from the P value followed by a linear ramp back up to the value of P. The modulated value of the FFD is always smaller than or equal to the value of P.

Figure 4. Spread Step and Period



The SS modulation period is defined as the amount of time steps it takes for the triangle to move from its lowest to its highest point. The period is essentially half of the modulation cycle or modulation rate. One time step is defined as one cycle of the output frequency FOUT. The period register setting needs to be half of the period decimal value, so essentially ¼ of the modulation cycle.

Period (decimal) = FPFD / (2×FSS) (6)

Period [11..0] = DEC2HEX(ROUND2INT(Period(decimal) / 2)) (7)

Given the required spread percentage and the period value, the step size is calculated as:

Step (decimal) = (SS% / 100) × P / Period (8)

Step [15..0] = DEC2HEX(ROUND2INT(224 × Step(decimal))) (9)

Example 1 with down spread (= default configuration):

FVCO = 2500MHz, FCLOCK = 100MHz with -0.5% down spread and 31.5kHz modulation rate.

The crystal is 25MHz and the doubler is enabled so FPFD = 25MHz × 2 = 50MHz.

FFD value P = (FVCO / (2 × FPFD)) = (2500 / (2×50)) = 25.

FOD integer [7..0] = DEC2HEX(25) = 19-hex.

FOD fraction [15..0] = DEC2HEX(ROUND2INT(216×0)) = DEC2HEX(ROUND2INT(0)) = 00 00 hex.

Period (decimal) = FPFD / (2×FSS) = 50 / (2×0.0315) = 793.6508.

Period [11:0] = DEC2HEX(ROUND2INT(Period(decimal) / 2)) = DEC2HEX(397) = 1 8D hex.

Step (decimal) = (SS% / 100) × P / Period = (0.5 / 100) × 25 / 793.6508 = 1.575 × 10-4.

Step [15..0] = DEC2HEX(ROUND2INT(224 × Step(decimal))) = DEC2HEX(2642) = 0A 42 hex.

Example 2 with center spread:

FVCO = 2430MHz, FOUT = 27MHz with ±1.0% center spread and 31.5kHz modulation rate.

The crystal is 25MHz and the doubler is enabled so FPFD = 25MHz × 2 = 50MHz.

FFD value P = (1 - SS% / 200) × (FVCO / (2 × FPFD)) = (1 + 2.0/200) × (2430 / (2×50)) = 1.01 × 24.3 = 24.543.

FFD integer [7..0] = DEC2HEX(24) = 18-hex.

FFD fraction [15..0] = DEC2HEX(ROUND2INT(216×0.543)) = DEC2HEX(ROUND2INT(35586.05)) = 8B 02 hex.

Period (decimal) = FOUT / (2×FSS) = 50 / (2×0.0315) = 793.6508.

Period [11:0] = DEC2HEX(ROUND2INT(Period(decimal) / 2)) = DEC2HEX(397) = 1 8D hex.

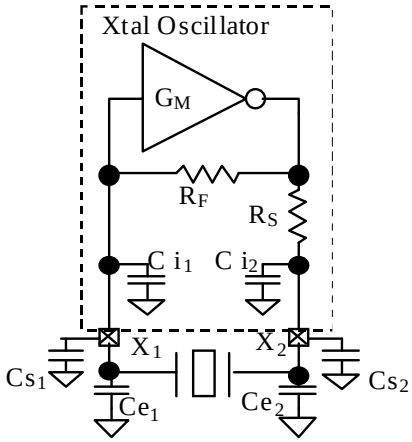
Step (decimal) = (SS% / 100) × P / Period = (2.0 / 100) × 24.543 / 793.6508 = 6.184836 × 10-4.

Step [15..0] = DEC2HEX(ROUND2INT(224 × Step(decimal))) = DEC2HEX(10376) = 28 88 hex.

Crystal Load Capacitance Registers

Registers 0x0E and 0x0F contain Crystal X1 and X2 Load capacitor settings that are used to add load capacitance to X1 and X2 (also known as XIN and XOUT) respectively.

Figure 5. Crystal Oscillator Circuit



Ci1 and Ci2 are on-chip capacitors that are programmable.

Cs is stray capacitance in the PCB and Ce is external capacitors for frequency fine tuning or for achieving load capacitance values beyond the range of the on-chip programmability. Consult the factory when adding Ce capacitors. The oscillator gain reduces with added capacitance and there may be crystal oscillator startup issues when adding too much capacitance.

All these capacitors combined make the load capacitance for the crystal.

Capacitance on pin XIN or X1: Cx1 = Ci1 + Cs1 + Ce1.
Capacitance on pin XOUT or X2: Cx2 = Ci2 + Cs2 + Ce2.
Total Crystal Load Capacitance C_L = Cx1 × Cx2 / (Cx1+Cx2).

For optimum balance and oscillator gain it is recommended to design Cx1 = Cx2. In that case C_L = Cx1 / 2 = Cx2 / 2.

The capacitance per pin X1 or X2 is: Cap (pF) = 7.98 + 0.442 × Bits[4..0] + 7.072 × Bit[5].

This includes an estimated Cs1 = Cs2 = 1.5pF.

When designing Cx1 = Cx2, the formula for CL is: C_L (pF) = 3.99+ 0.221 × Bits[4..0] + 3.536 × Bit[5].

The minimum C_L value at Cx1 = Cx2 = '00 0000'-binary = 3.99pF.
The maximum C_L value at Cx1 = Cx2 = '11 1111'-binary = 3.99 + 0.221 × 31 + 3.536 × 1 = 14.38pF (not counting Ce).

Example: For a crystal C_L of 8pF, the registers can be programmed as follows:

C_L (pF) = 3.99 + 0.221 × 18 + 3.536 × 0 = 7.97pF (nearest to 8.0pF).

So for C_L = 8pF the recommended settings are Cx1[5..0] = Cx2[5..0] = 18 or '01 0010'-binary.

Registers 0x0E = 0x0F = 92-hex (= '1001 0010' binary).

Note about precision: The above formulas use 0.001pF resolution. This is to keep the calculations consistent. The actual accuracy is, at best, 0.1pF due to process variations in the PCB and the 9FGV1006 chip.

Revision History

Revision Date	Description of Change
October 20, 2017	Initial release.

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