



Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 96138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: M1806-01 DATE: June 15, 2018 Product Affected: TSE2004GB2B0NCG8, TSE2004GB2B0NCG8/B, TSE2004GB2B0NCG8/M Date Effective: September 15, 2018	MEANS OF DISTINGUISHING CHANGED DEVICES: <input checked="" type="checkbox"/> Product Mark Change in the top mark and orderable part# <input type="checkbox"/> Back Mark <input type="checkbox"/> Date Code <input type="checkbox"/> Other
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Contact: IDT PCN DESK E-mail: pcndesk@idt.com	Attachment: <input checked="" type="checkbox"/> Yes <input type="checkbox"/> No Samples: Available
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DESCRIPTION AND PURPOSE OF CHANGE:

<input type="checkbox"/> Die Technology <input type="checkbox"/> Wafer Fabrication Process <input type="checkbox"/> Assembly Process <input type="checkbox"/> Equipment <input type="checkbox"/> Material <input type="checkbox"/> Testing <input checked="" type="checkbox"/> Manufacturing Site <input type="checkbox"/> Data Sheet <input type="checkbox"/> Other	<p>This notification is to advise our customer that IDT is transferring the wafer fab production currently manufactured in Global Foundry (GF) to Semiconductor Manufacturing International Corporation (SMIC).</p> <p>SMIC will closely match the GF process for the products transfer.</p> <p>There is no expected change to the data sheet, package or backend manufacturing process.</p> <p>There will be change in the top mark and ordering part number as shown in the below table. The current part will be discontinued as of the effective date of this PCN.</p> <p>Refer to Attachment for qualification report.</p> <table border="1" style="margin-left: auto; margin-right: auto; border-collapse: collapse; text-align: center;"> <thead> <tr style="background-color: #cccccc;"> <th style="padding: 5px;">Current Part# (GF)</th> <th style="padding: 5px;">New Part# (SMIC)</th> </tr> </thead> <tbody> <tr> <td style="padding: 5px;">TSE2004GB2B0NCG8</td> <td style="padding: 5px;">TSE2004GB2C0NCG8</td> </tr> <tr> <td style="padding: 5px;">TSE2004GB2B0NCG8/B</td> <td style="padding: 5px;">TSE2004GB2C0NCG8/B</td> </tr> <tr> <td style="padding: 5px;">TSE2004GB2B0NCG8/M</td> <td style="padding: 5px;">TSE2004GB2C0NCG8/M</td> </tr> </tbody> </table>	Current Part# (GF)	New Part# (SMIC)	TSE2004GB2B0NCG8	TSE2004GB2C0NCG8	TSE2004GB2B0NCG8/B	TSE2004GB2C0NCG8/B	TSE2004GB2B0NCG8/M	TSE2004GB2C0NCG8/M
Current Part# (GF)	New Part# (SMIC)								
TSE2004GB2B0NCG8	TSE2004GB2C0NCG8								
TSE2004GB2B0NCG8/B	TSE2004GB2C0NCG8/B								
TSE2004GB2B0NCG8/M	TSE2004GB2C0NCG8/M								

RELIABILITY/QUALIFICATION SUMMARY:

Wafer and Component level Qualification and Characterization tests will verify that there is no change to the performance or reliability of the product.

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.

IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: _____ Name/Date: _____ Title: _____	<input type="checkbox"/> <i>Approval for shipments prior to effective date.</i> E-Mail Address: _____ Phone# /Fax# : _____
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CUSTOMER COMMENTS: _____

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____ **DATE:** _____



Integrated Device Technology, Inc.

Qualification Test Result Summary

Product: TSE2004GB2C0NCG

Foundry: SMIC

Technology Information: CE018 2P4M

Package Family: VFQFP-N

Qual Test Result Summary - JESD47 Recommended Tests

Test Description	Conditions	Sample Size	Rejects	Comments
High Temperature Operating Life (Dynamic)	JESD22-A108, +125°C, Vccmax @ 1000 hours or equivalent	77 77 77	0 0 0	
ESD: Human Body Model	JS-001	3	0	2000V
ESD: Charged Device Model	JESD22-C101	3	0	500V
Latch-Up	JESD78	6	0	
Electrical Characterization	Per Datasheet	10*	-	Passed
Elevated Temp NV Cycling Endurance (NVCE)	JESD22-A117 100K cycles @ 85C VCC= Max	77 77 77	0 0 0	
EEPROM Data Retention - High Temperature (HTDR)	JESD22-A117 150C/1000hrs	39 39 39	0 0 0	Samples have been subjected to 100K Elevated Temp NVCE

Note: * Sample size applies to base characterization



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Qualification Test Result Summary

Qualification Test Result Summary – JESD47 Recommended Tests

Test /Conditions	Conditions	Sample Size	Rejects	Comments
Room Temp NV Cycling Endurance (NVCE)	JESD22-A117 100K cycles @ 25C VCC= Max	77 77 77	0 0 0	
EEPROM Data Retention - High Temperature (HTDR*)	JESD22-A117 150C/1000hrs	77 77 77	0 0 0	*Samples have been subjected to 100K Room Temp NVCE
EEPROM Data Retention - High Temperature (HTDR) - Wafer Level*	JESD22-A117 250degC Bake/ 70hrs	1 1 1	0 0 0	To guarantee 10yrs/ 125C based on SMIC process activation energy
Temperature Cycle	JESD22-A104D, -55°C to +125°C, 700 cycles	25 25 25	0 0 0	
High Temperature Storage Bake	JESD22-A-103D, 150°C, 1000 hrs	25 25 25	0 0 0	
Highly Accelerated Stress Test (HAST)	EIA/JESD22-A110D, 130°C/85%R.H. Vcc max for 96 hours	25 25 25	0 0 0	
Moisture Classification	J-STD-020C	25 25	0 0	
Physical Dimensions	JESD22-B100 (Per applicable IDT Package Outline Drawing)	30 30 30	0 0 0	
Solderability Test	JESD22-B102-C, MIL-STD-883 (Method 2003)	5 ¹ 5 ² 5 ³	0 0 0	¹ Sn/Pb 215°C/5sec ² Sn/Pb 245°C/5sec ³ Sn 245°C/5sec

Note: For MSL, HAST and Temperature Cycle, samples have been subjected to pre-conditioning per JESD22-A113

Qualification Test Result Summary

Qualification Test Result Summary – JESD47 Recommended Tests

Test /Conditions	Conditions	Sample Size	Rejects	Comments
Ball Shear Test	EIA/JESD22-B116 (IDT Spec MAA-3057)	5	0	Note 1
		5	0	
		5	0	
Bond Pull Test	IPC-TM-650 (IDT Spec MAC-3010)	5	0	Note 1
		5	0	
		5	0	

Note-1: Sub-con data