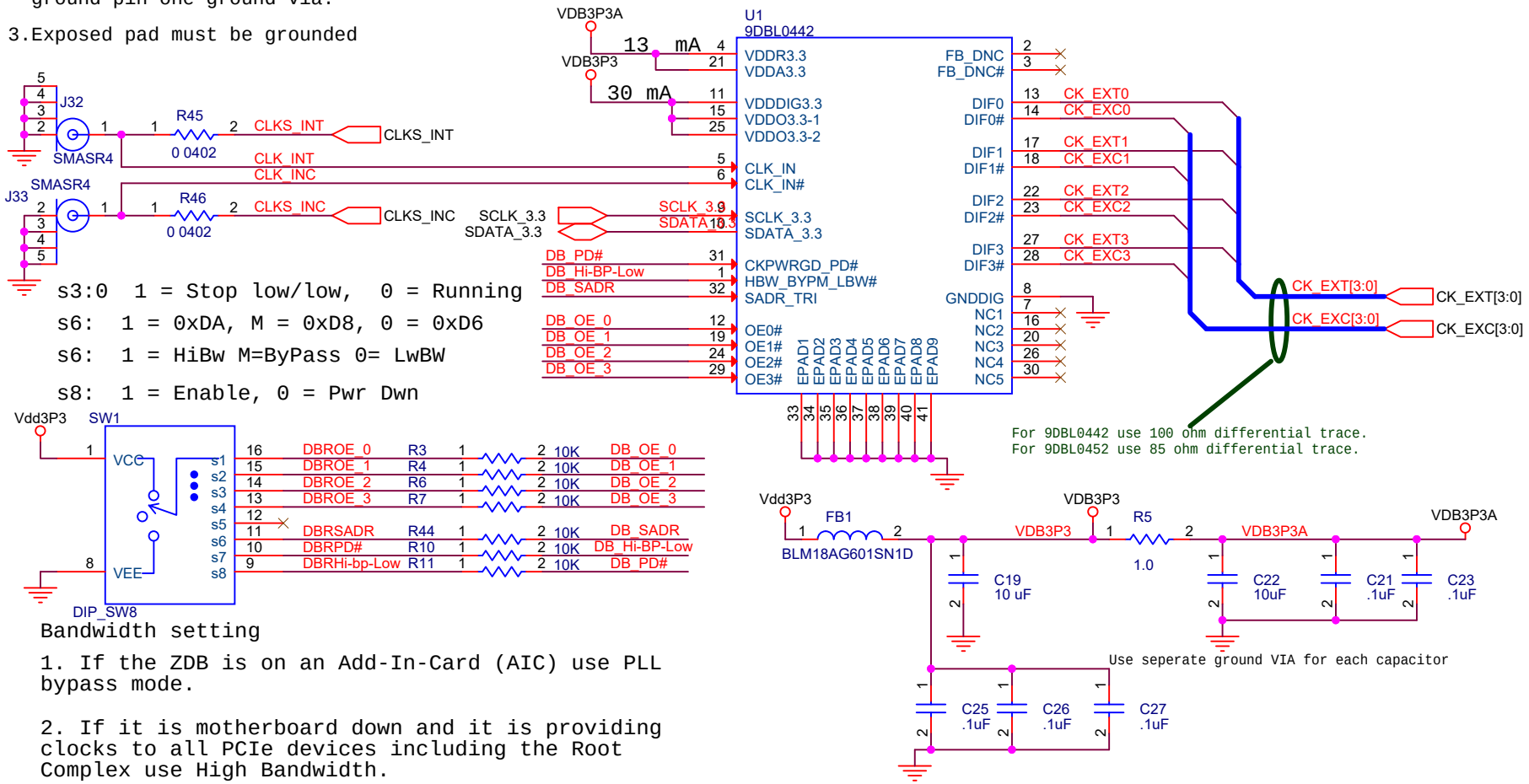
**Layout notes.**

1. Route power from bead through bulk capacitor pad then through 0.1uF capacitor pad then to clock chip Vdd pad.
2. Do not share ground vias. One ground pin one ground via.

3. Exposed pad must be grounded




s3:0 1 = Stop low/low, 0 = Running

s6: 1 = 0xDA, M = 0xD8, 0 = 0xD6

s6: 1 = HiBw M=ByPass 0= LwBW

s8: 1 = Enable, 0 = Pwr Dwn

For 9DBL0442 use 100 ohm differential trace.
For 9DBL0452 use 85 ohm differential trace.







Bandwidth setting

1. If the ZDB is on an Add-In-Card (AIC) use PLL bypass mode.

2. If it is motherboard down and it is providing clocks to all PCIe devices including the Root Complex use High Bandwidth.

NOTE:FERRITE BEADS FB1 =

| Manufacture | Part Number | Z@100MHz | PkgSz | DC res. | Current(Ma) |
|---|---|---|---|---|---|
| muRata | BLM21AG60SN1 | 600 | 0805 | 0.30 | 600 |
| TDK | MMZ2012S601A | 600 | 0805 | 0.30 | 600 |
| STEWARD | HZ0805E601R | 600 | 0805 | 0.30 | 600 |
| AssocCmpTch | CBG0805-600-50 | 600 | 0805 | 0.30 | 600 |

| Manufacture | Part Number | Z@100MHz | PkgSz | DC res. | Current(Ma) |
|---|---|---|---|---|---|
| muRata | BLM18AG601SN1 | 600 | 0603 | 0.50 | 200 |
| muRata | BLM18BD601SN1_PB | 600 | 0603 | 0.65 | 200 |
| Ceratech | HB-1T1608-601 | 600 | 0603 | 0.50 | 200 |
| TDK | MMZ1608R301A | 300 | 0603 | 0.20 | 500 |

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| Size | Document Number | Rev |
|---|---|---|
| A | 9DBL0442B_EVB | 0.3 |

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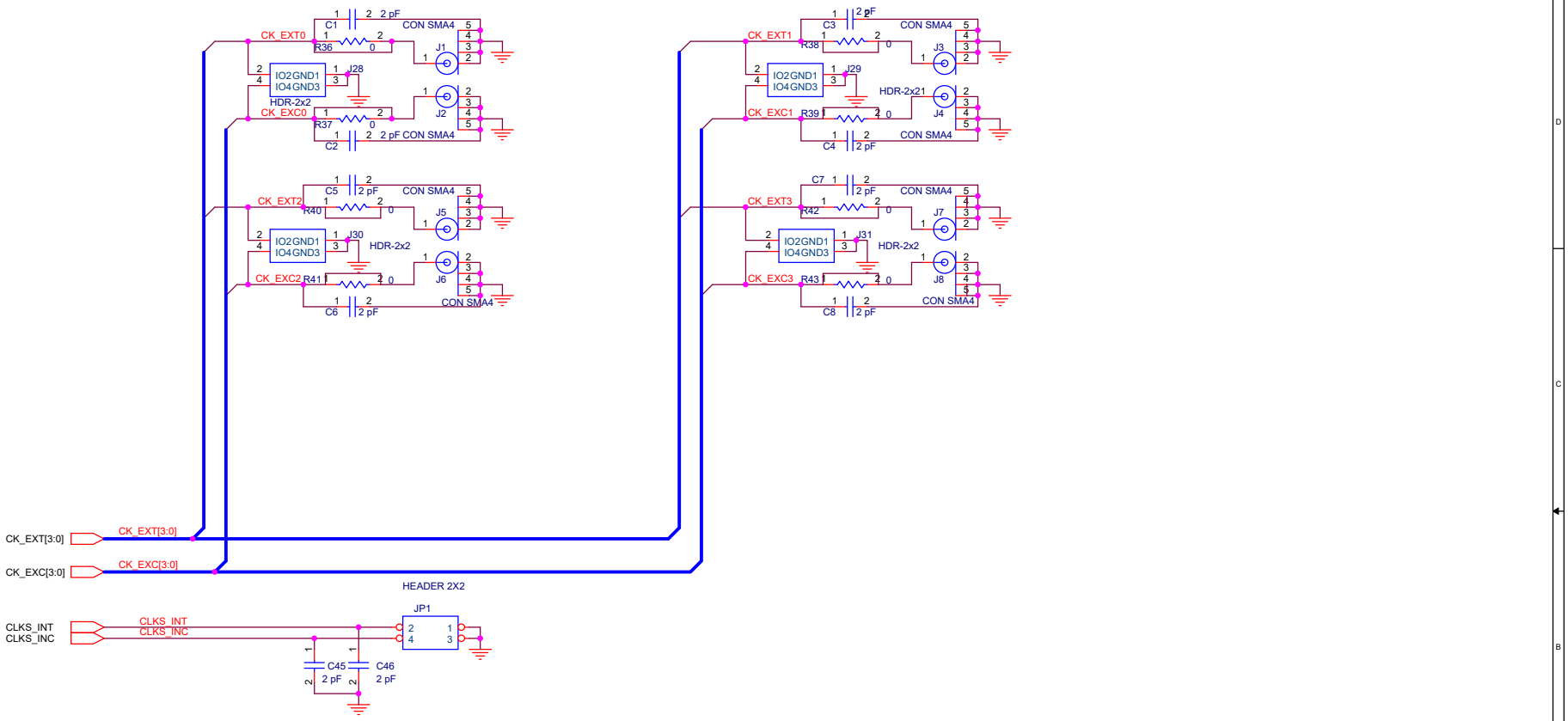


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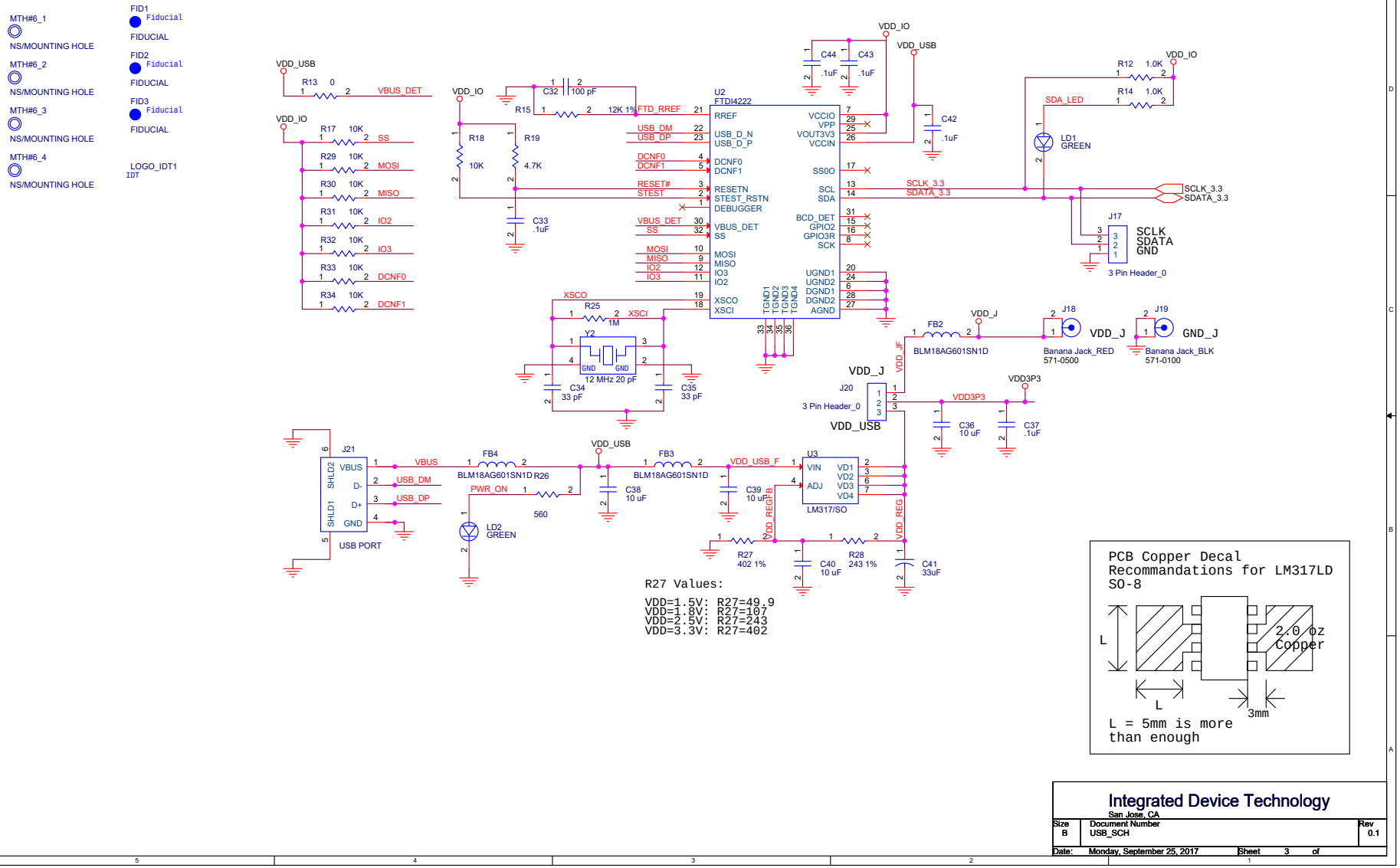
|---|---|---|
| Title | <Title> | |
| Size B | Document Number <Doc> | Rev <RevCode> |
| Date: Monday, September 25, 2017 | Sheet 2 of 3 | |

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| Size: B | Document Number: USB_SCH | Rev: 0.1 |
| Date: Monday, September 25, 2017 | Sheet 3 of | |