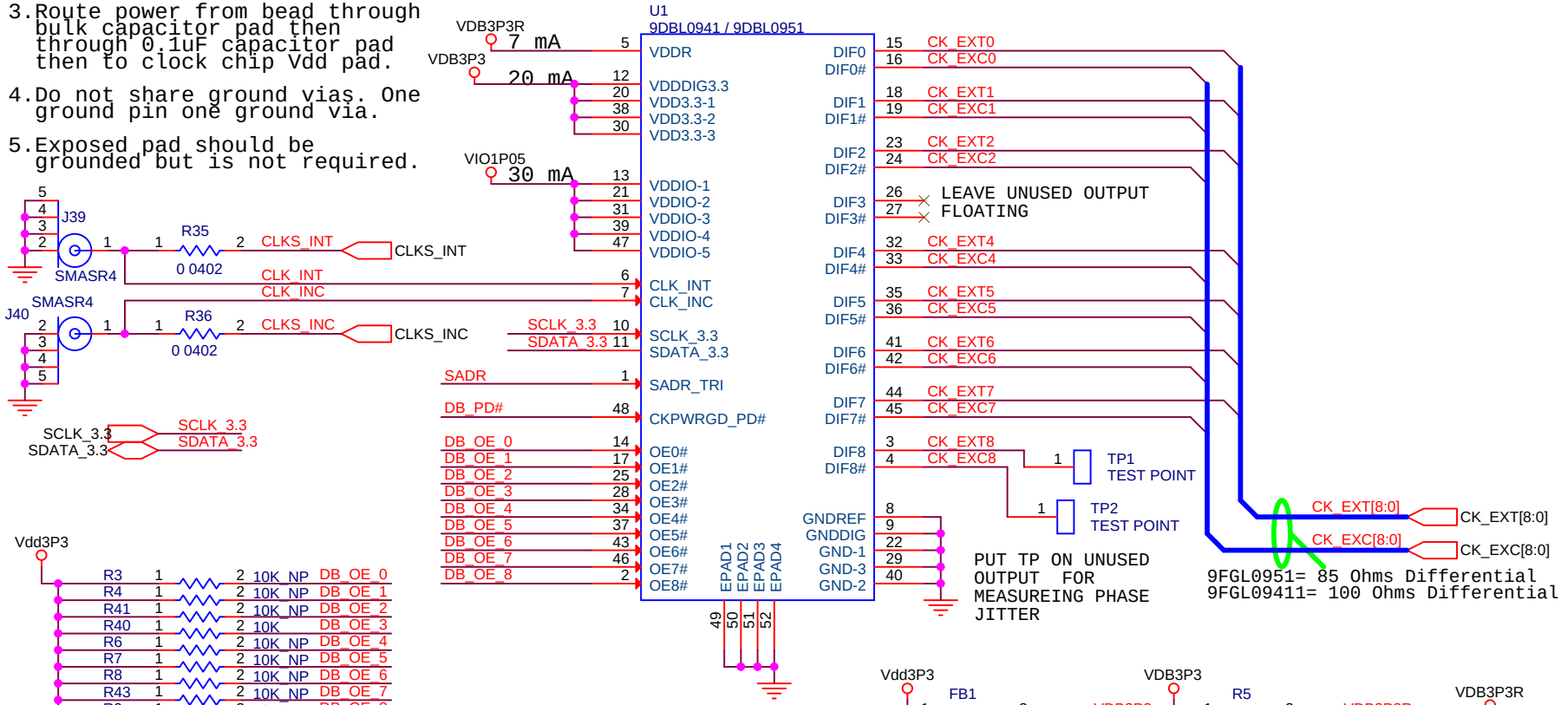
Layout notes.

3.Route power from bead through bulk capacitor pad then through 0.1uF capacitor pad then to clock chip Vdd pad.

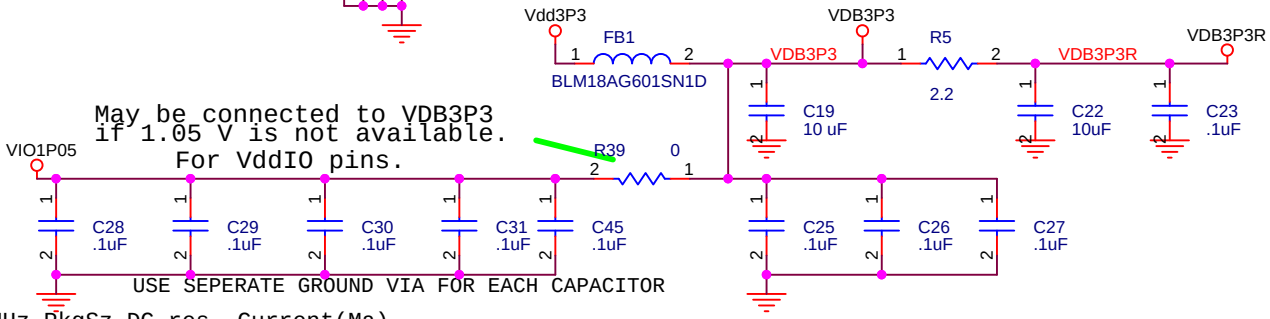
4.Do not share ground vias. One ground pin one ground via.

5.Exposed pad should be grounded but is not required.










NOTE:FERRITE BEADS FB1 =

| Manufacture | Part Number | Z@100MHz | PkgSz | DC res. | Current(Ma) |
|---|---|---|---|---|---|
| muRata | BLM21A6G01SN1 | 600 | 0805 | 0.30 | 600 |
| TDK | MMZ2012S601A | 600 | 0805 | 0.30 | 600 |
| STEWARD | HZ0805E601R | 600 | 0805 | 0.30 | 600 |
| AssocCmpTch | CBG0805-600-50 | 600 | 0805 | 0.30 | 600 |

| Manufacture | Part Number | Z@100MHz | PkgSz | DC res. | Current(Ma) |
|---|---|---|---|---|---|
| muRata | BLM18AG601SN1 | 600 | 0603 | 0.50 | 200 |
| muRata | BLM18BD601SN1_PB | 600 | 0603 | 0.65 | 200 |
| Ceratech | HB-1T1608-601 | 600 | 0603 | 0.50 | 200 |
| TDK | MMZ1608R301A | 300 | 0603 | 0.20 | 500 |

Integrated Device Technology
San Jose, CA

| Size | Document Number | Rev |
|---|---|---|
| A | 9DBL0941/9DBL0851 | 0.2 |

Date: Thursday, September 07, 2017 Sheet 1 of 3