



Integrated Device Technology, Inc.  
2975 Stender Way, Santa Clara, CA - 95054

## PRODUCT/PROCESS CHANGE NOTICE (PCN)

<p>PCN #: SM-0112-03                      DATE: 12/24/01</p> <p>Product Affected: 64K, 72K, 128K and 144K Dual-Port Family (refer to attached List for product details)</p> <p>Manufacturing Location Affected: N/A</p> <p>Date Effective: 3/23/02</p>	<p>MEANS OF DISTINGUISHING CHANGED DEVICES:</p> <p><input checked="" type="checkbox"/> Product Mark            Die Revision "U" on Top Mark</p> <p><input type="checkbox"/> Back Mark</p> <p><input type="checkbox"/> Date Code</p> <p><input type="checkbox"/> Other</p>
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<p>Contact: George Snell</p> <p>Title: Quality Assurance Manager</p> <p>Phone #: (831) 754-4556</p> <p>Fax #: (831) 754-4672</p> <p>E-mail: <a href="mailto:george.snell@idt.com">george.snell@idt.com</a></p>	<p>Attachment:                      <input checked="" type="checkbox"/> Yes                      <input type="checkbox"/> No</p> <p>Samples: Available upon request. Please contact your local Sales Representative for schedule.</p>
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**DESCRIPTION AND PURPOSE OF CHANGE:**

<ul style="list-style-type: none"> <li><input checked="" type="checkbox"/> Die Technology</li> <li><input checked="" type="checkbox"/> Wafer Fabrication Process</li> <li><input type="checkbox"/> Assembly Process</li> <li><input type="checkbox"/> Equipment</li> <li><input type="checkbox"/> Material</li> <li><input type="checkbox"/> Testing</li> <li><input checked="" type="checkbox"/> Manufacturing Site</li> <li><input type="checkbox"/> Data Sheet</li> <li><input type="checkbox"/> Other</li> </ul>	<p>This change is to upgrade to a new technology (CMOS9) and shrink die. This change is to improve manufacturability and allow for expanded product offerings.</p>
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**RELIABILITY/QUALIFICATION SUMMARY:**

Qualification testing will verify that there is no change to the product reliability. Qualification details are available upon request

**CUSTOMER ACKNOWLEDGMENT OF RECEIPT:**

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.

**IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.**

Customer: _____	<input type="checkbox"/> <i>Approval for shipments prior to effective date.</i>
Name/Date: _____	E-Mail Address: _____
Title: _____	Phone# /Fax# : _____

**CUSTOMER COMMENTS:** \_\_\_\_\_

**IDT ACKNOWLEDGMENT OF RECEIPT:**

RECD. BY: \_\_\_\_\_                      DATE: \_\_\_\_\_



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### ATTACHMENT - PCN #: SM-0112-03

**PCN Summary**

**PCN Type:** Mask/Design Change for Die Shrink

**Commodity** Memory

**Forecast or Execute** Execute

**Planned or Unplanned** Planned

**Data Sheet Change** N/A

**Detail of Change**

The base device for each part is detailed on the attached product detail sheet. The new base device for future products listed on this PCN will be 7025 "U". This product redesign will allow for IDT to expand product offerings and upgrade technology. The Hillsboro, Oregon Wafer Fabrication Facility has been previously qualified for CMOS 9 processing.

Base Device / Die Revision	Current Die Revision		Planned Change	
	7025V	70V25V	7025U	70V25U
Wafer Fab Facility	Salinas, CA	Salinas, CA	Hillsboro, OR	Hillsboro, OR
Wafer Fab Technology	CMOS 8	CMOS 8	CMOS 9	CMOS 9
Wafer Size	6 inch	6 inch	8 inch	8 inch
# Poly Layers	2	2	3	3
# Metal Layers	2	2	2	2
Minumum Feature Size / $\mu\text{m}$	0.6	0.4	0.55	0.32
Die Dimensions/(K sq mils)	39.6K	39.6K	32K	32K

**Conversion schedule :** Shown on attached Product listing on page 4 .



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#### Qualification Plan:

Test Vehicles	Required Sample / # Fails	Expected Completion Date			
		1/31/2002	3/4/2002	5/4/2002	6/15/2002
<b>70V25U (3.3V) &amp; 7025U (5V)</b>		LOT #1 3.3V	LOT #2 3.3V	LOT #1 5V	LOT #2 5V
Operating Life Test: Dynamic @+135°C, Vcc=6V for 750 hours or Vcc=4V for 750 hours	116 / 0				
High Temp. Storage Life Test (Unbiased, 1000 hours @+150°C)	77 / 0				
Bake & Ballshear Test @ 200°C / 4 ball bonds per device	5 / 0				
Temperature Cycling: ( -65°C to +150°C, 500 cycles)	45 / 0				
HAST: (Biased, 100 Hrs. @+130°C, +85%RH, 3 Atm.)	45 / 0				
Autoclave:(Unbiased, 2 Atm Saturated Steam, +121°C, 168 Hrs)	45 / 0				
ESD Human Body Model	6 / 0				
ESD Charged Device Model	6 / 0				
Latch up: ( Tested to 2X Vcc)	10 / 0				

Tests are completed for unshaded areas. Product released is based on qualification of initial lot.



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IDT7025 Family of Parts										
Part Number	Old Rev.	New Rev.	New Speed Grades	Interface	Vcc	Bus	Depth	Density	Sample Availability	Production Availability
IDT7035S/L	V	U	10, 12 ns	Async	5	x18	8K	144K	March 2002	May 2002
IDT7034S/L	V	U	10, 12 ns	Async	5	x18	4K	72K	March 2002	May 2002
IDT7025S/L	V	U	10, 12 ns	Async	5	x16	8K	128K	March 2002	May 2002
IDT7024S/L	V	U	10, 12 ns	Async	5	x16	4K	64K	March 2002	May 2002
IDT7016S/L	V	U	10, 12 ns	Async	5	x9	16K	144K	April 2002	May 2002
IDT7015S/L	V	U	10, 12 ns	Async	5	x9	8K	72K	April 2002	May 2002
IDT7016S/L	W	U	10, 12 ns	Async	5	x9	16K	144K	April 2002	May 2002
IDT7015S/L	W	U	10, 12 ns	Async	5	x9	8K	72K	April 2002	May 2002
IDT7006S/L	V	U	10, 12 ns	Async	5	x8	16K	128K	April 2002	May 2002
IDT7005S/L	V	U	10, 12 ns	Async	5	x8	8K	64K	April 2002	May 2002
IDT70V35S/L	V	U	10, 12 ns	Async	3.3	x18	8K	144K	January 2002	February 2002
IDT70V34S/L	V	U	10, 12 ns	Async	3.3	x18	4K	72K	January 2002	February 2002
IDT70V25S/L	V	U	10, 12 ns	Async	3.3	x16	8K	128K	January 2002	February 2002
IDT70V24S/L	V	U	10, 12 ns	Async	3.3	x16	4K	64K	January 2002	February 2002
IDT70V06S/L	V	U	10, 12 ns	Async	3.3	x8	16K	128K	February 2002	March 2002
IDT70V05S/L	V	U	10, 12 ns	Async	3.3	x8	8K	64K	February 2002	March 2002