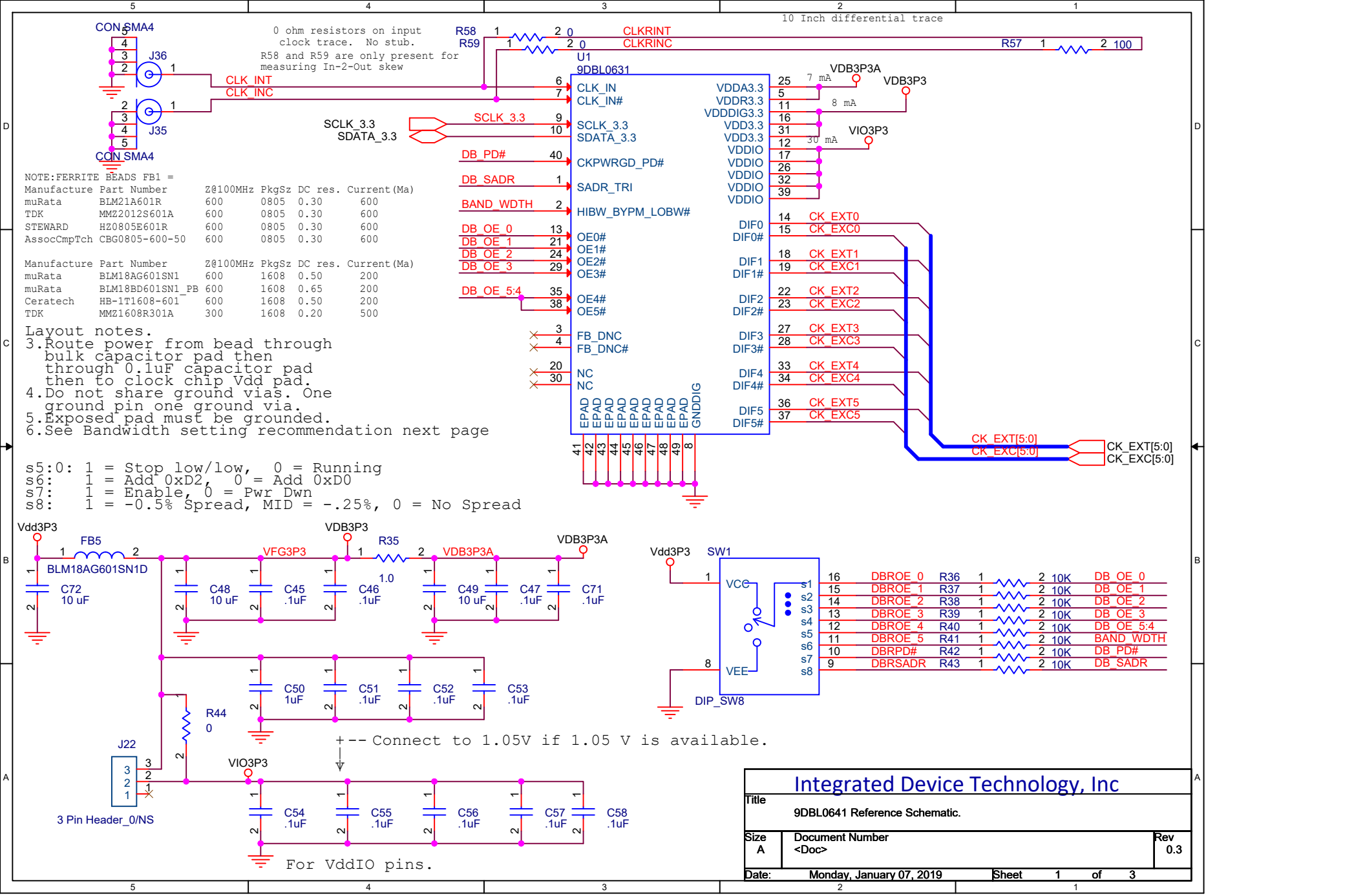
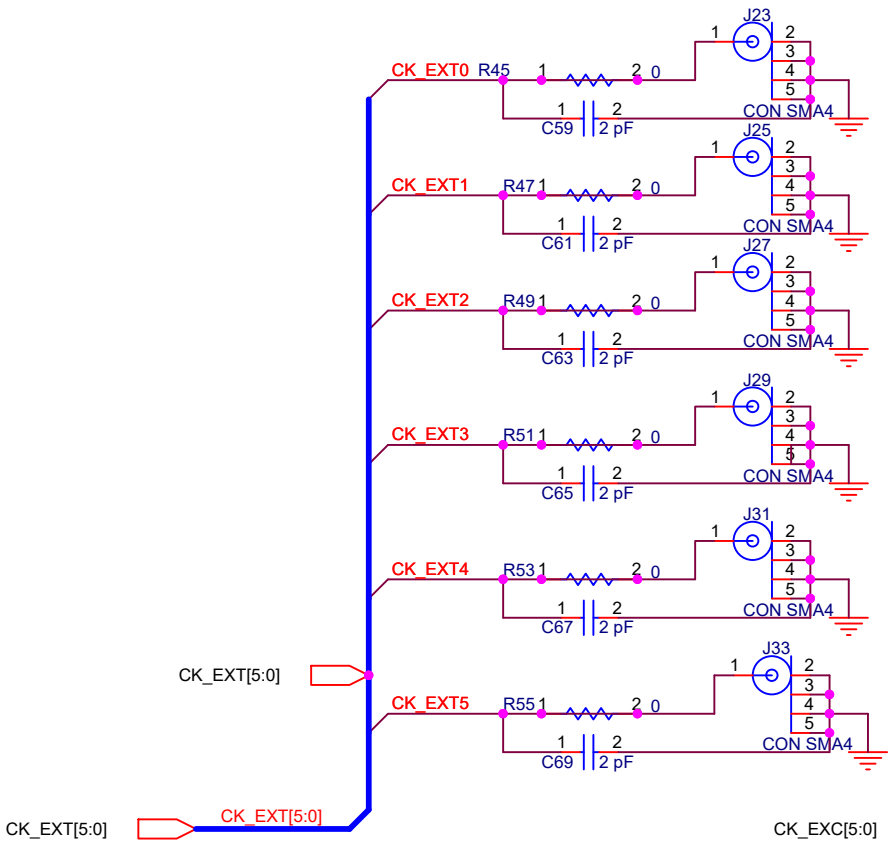
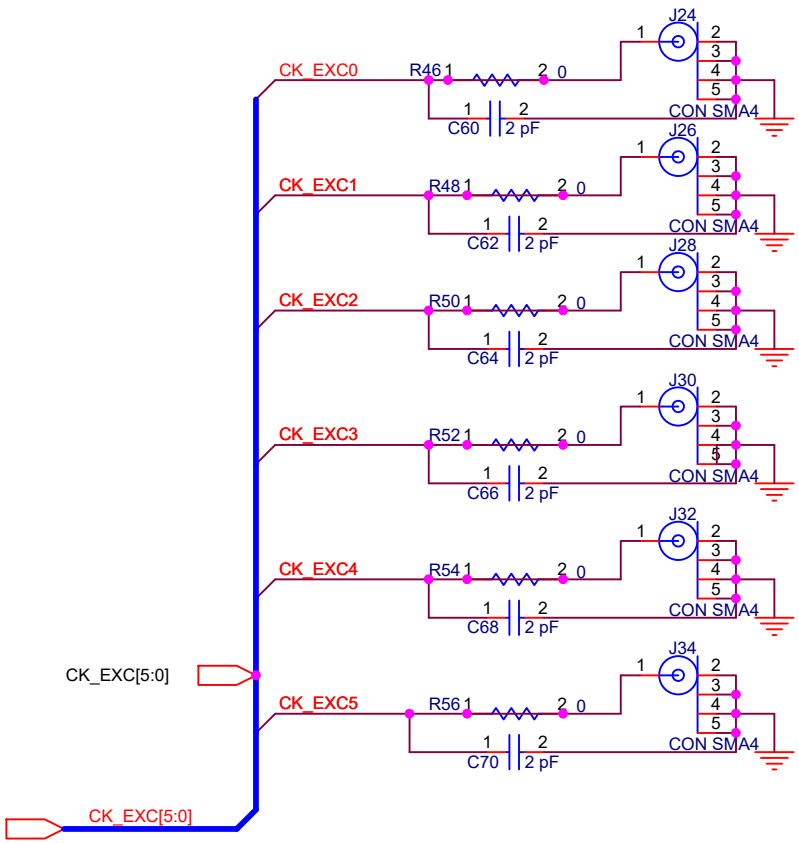

10 Inch differential trace
CON SMA4
J36
J35
CON SMA4
CLK_INT
CLK_INC
0 ohm resistors on input clock trace. No stub.
R58 and R59 are only present for measuring In-2-Out skew
R58
R59
CLKRINT
CLKRINC
R57 100
U1
9DBL0631
SCLK_3.3
SDATA_3.3
DB_PD#
DB_SADR
BAND_WDTH
DB_OE_0
DB_OE_1
DB_OE_2
DB_OE_3
DB_OE_5:4
CLK_IN
CLK_IN#
SCLK_3.3
SDATA_3.3
CKPWRGD_PD#
SADR_TRI
HIBW_BYPM_LOBW#
OE0#
OE1#
OE2#
OE3#
OE4#
OE5#
FB_DNC
FB_DNC#
NC
NC
EPAD
GNDDIG
VDDA3.3
VDDR3.3
VDDDIG3.3
VDD3.3
VDD3.3
VDDIO
DIF0
DIF0#
DIF1
DIF1#
DIF2
DIF2#
DIF3
DIF3#
DIF4
DIF4#
DIF5
DIF5#
VDB3P3A
7 mA
VDB3P3
8 mA
VIO3P3
30 mA
CK_EXT0
CK_EXC0
CK_EXT1
CK_EXC1
CK_EXT2
CK_EXC2
CK_EXT3
CK_EXC3
CK_EXT4
CK_EXC4
CK_EXT5
CK_EXC5
CK_EXT[5:0]
CK_EXC[5:0]
NOTE:FERRITE BEADS FB1 =
Manufacture Part Number Z@100MHz PkgSz DC res. Current(Ma)
muRata BLM21A601R 600 0805 0.30 600
TDK MMZ2012S601A 600 0805 0.30 600
STEWARD HZ0805E601R 600 0805 0.30 600
AssocCmpTch CBG0805-600-50 600 0805 0.30 600
Manufacture Part Number Z@100MHz PkgSz DC res. Current(Ma)
muRata BLM18AG601SN1 600 1608 0.50 200
muRata BLM18BD601SN1_PB 600 1608 0.65 200
Ceratech HB-1T1608-601 600 1608 0.50 200
TDK MMZ1608R301A 300 1608 0.20 500
Layout notes.
3.Route power from bead through bulk capacitor pad then through 0.1uF capacitor pad then to clock chip Vdd pad.
4.Do not share ground vias. One ground pin one ground via.
5.Exposed pad must be grounded.
6.See Bandwidth setting recommendation next page
s5:0: 1 = Stop low/low, 0 = Running
s6: 1 = Add 0xD2, 0 = Add 0xD0
s7: 1 = Enable, 0 = Pwr Dwn
s8: 1 = -0.5% Spread, MID = -.25%, 0 = No Spread
Vdd3P3
FB5
BLM18AG601SN1D
C72 10 uF
VFG3P3
C48 10 uF
C45 .1uF
C46 .1uF
VDB3P3
R35
1.0
VDB3P3A
C49 10 uF
C47 .1uF
C71 .1uF
C50 1uF
C51 .1uF
C52 .1uF
C53 .1uF
R44 0
J22
3 Pin Header_0/NS
+-- Connect to 1.05V if 1.05 V is available.
VIO3P3
C54 .1uF
C55 .1uF
C56 .1uF
C57 .1uF
C58 .1uF
For VddIO pins.
Vdd3P3
SW1
VCC
VEE
DIP_SW8
DBROE_0 R36 10K DB_OE_0
DBROE_1 R37 10K DB_OE_1
DBROE_2 R38 10K DB_OE_2
DBROE_3 R39 10K DB_OE_3
DBROE_4 R40 10K DB_OE_5:4
DBROE_5 R41 10K BAND_WDTH
DBRPD# R42 10K DB_PD#
DBRSADR R43 10K DB_SADR
Integrated Device Technology, Inc
Title
9DBL0641 Reference Schematic.
Size A
Document Number <Doc>
Rev 0.3
Date: Monday, January 07, 2019
Sheet 1 of 3



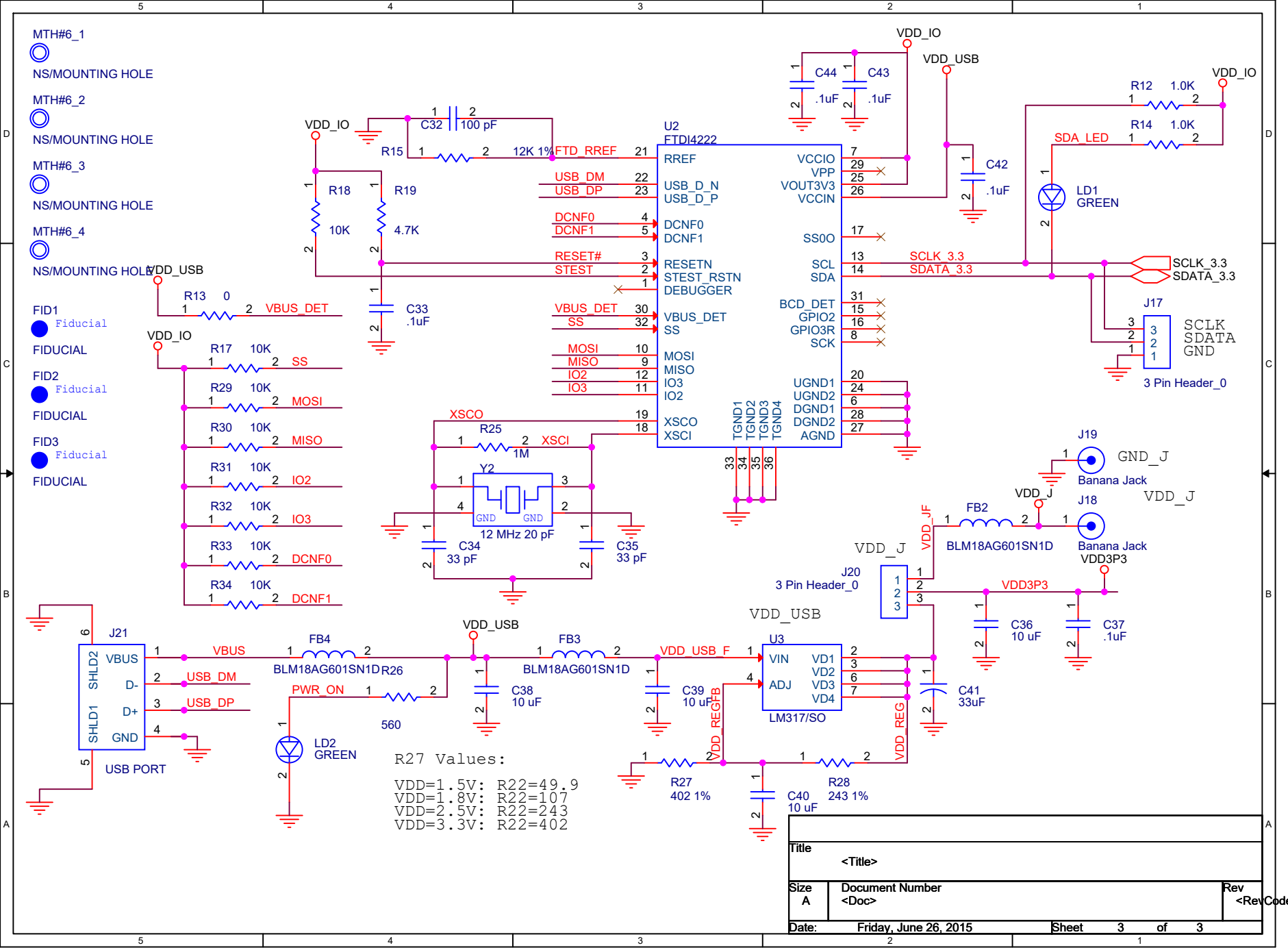


Bandwidth setting

1. If the ZDB is on an Add-In-Card (AIC) use PLL bypass mode.

2. If it is motherboard down and it is providing clocks to all PCIe devices including the Root Complex use High Bandwidth.

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, January 07, 2019	Sheet 2 of 3	


MTH#6_1
NS/MOUNTING HOLE
MTH#6_2
NS/MOUNTING HOLE
MTH#6_3
NS/MOUNTING HOLE
MTH#6_4
NS/MOUNTING HOLE
FID1
Fiducial
FIDUCIAL
FID2
Fiducial
FIDUCIAL
FID3
Fiducial
FIDUCIAL
U2
FTDI4222
VDD_IO
VDD_USB
C32 100 pF
R15 12K 1%
FTD_RREF
R18 10K
R19 4.7K
C33 .1uF
C44 .1uF
C43 .1uF
C42 .1uF
R12 1.0K
R14 1.0K
SDA_LED
LD1 GREEN
USB_DM
USB_DP
DCNF0
DCNF1
RESET#
STEST
VBUS_DET
SS
MOSI
MISO
IO2
IO3
XSCO
XSCI
SCLK_3.3
SDATA_3.3
J17
SCLK
SDATA
GND
3 Pin Header_0
R13 0
R17 10K
R29 10K
R30 10K
R31 10K
R32 10K
R33 10K
R34 10K
R25 1M
Y2
12 MHz 20 pF
C34 33 pF
C35 33 pF
J19
GND_J
Banana Jack
VDD_J
J18
FB2
BLM18AG601SN1D
VDD_JF
J20
3 Pin Header_0
VDD3P3
C36 10 uF
C37 .1uF
J21
USB PORT
VBUS
FB4
BLM18AG601SN1D
R26
PWR_ON
560
LD2 GREEN
C38 10 uF
FB3
BLM18AG601SN1D
VDD_USB_F
U3
LM317/SO
C39 10 uF
C41 33uF
VDD_REGFB
VDD_REG
R27 402 1%
R28 243 1%
C40 10 uF
R27 Values:
VDD=1.5V: R22=49.9
VDD=1.8V: R22=107
VDD=2.5V: R22=243
VDD=3.3V: R22=402
Title
<Title>
Size A
Document Number
<Doc>
Rev
<RevCode>
Date: Friday, June 26, 2015
Sheet 3 of 3