Layout notes.

1. Separate Xout and Xin traces by at least 3 x the trace width.
2. Do not share crystal load capacitor ground via with other components.
3. Route power from bead through bulk capacitor pad then through 0.1uF capacitor pad then to clock chip Vdd pad.
4. Do not share ground vias. One ground pin one ground via.
5. Exposed pad should be grounded but is not required.

U1
9FGL0841

VFG3P3A 7 mA
VFG3P3 8 mA
20 mA
VIO3P3 30 mA

VDDA3.3, VDDREF3.3, VDDXTAL3.3, VDDDIG3.3, VDD3.3-1, VDD3.3-2, VDDIO-1, VDDIO-2, VDDIO-3, VDDIO-4, VDDIO-5

SADR/REF3.3, DIF0, DIF0#, DIF1, DIF1#, DIF2, DIF2#, DIF3, DIF3#, DIF4, DIF4#, DIF5, DIF5#, DIF6, DIF6#, DIF7, DIF7#

CKR_REF, CK_EXT0, CK_EXC0, CK_EXT1, CK_EXC1, CK_EXT2, CK_EXC2, CK_EXT3, CK_EXC3, CK_EXT4, CK_EXC4, CK_EXT5, CK_EXC5, CK_EXT6, CK_EXC6, CK_EXT7, CK_EXC7

GNDXTAL, GNDREF, GNDDIG, GND-1, GNDA, GND-2

EPAD1, EPAD2, EPAD3, EPAD4

SMB_ADD — R36 10K — CK_REF
R1 33 — CK_REF

Y1 25 MHz 8 pF
C9 6.8 pF
C12 6.8 pF
GND GND GND

FG_X1, FG_X2, X1_25, X2
SCLK_3.3, SDATA_3.3
FG_SS_EN, SS_EN_TRI
FG_PD#, CKPWRGD_PD#
FG_OE_0, FG_OE_1, FG_OE_3:2, FG_OE_5:4, FG_OE_7:6
OE0#, OE1#, OE2#, OE3#, OE4#, OE5#, OE6#, OE7#

SMA2S J23, C46 2 pF
J1 CK_EXT0, C1 2 pF
J2 CK_EXC0, C2 2 pF
J3 CK_EXT1, C3 2 pF
J4 CK_EXC1, C4 2 pF
J5 CK_EXT2, C5 2 pF
J6 CK_EXC2, C6 2 pF
J7 CK_EXT3, C7 2 pF
J8 CK_EXC3, C8 2 pF
J9 CK_EXT4, C10 2 pF
J10 CK_EXC4, C11 2 pF
J11 CK_EXT5, C13 2 pF
J12 CK_EXC5, C14 2 pF
J13 CK_EXT6, C15 2 pF
J14 CK_EXC6, C16 2 pF
J15 CK_EXT7, C17 2 pF
J16 CK_EXC7, C18 2 pF

Test load

s5:0 1 = Stop low/low, 0 = Running
s6: 1 = Add 0xD4, 0 = Add 0xD0
s7: 1 = Enable, 0 = Pwr Dwn
s8: 1 = -0.5% Spread, MID = -.25%, 0 = No Spread

Vdd3P3 SW1 DIP_SW8
VCC, VEE, s1–s8

FGROE_0 R3 10K FG_OE_0
FGROE_1 R4 10K FG_OE_1
FGROE_3:2 R6 10K FG_OE_3:2
FGROE_5:4 R7 10K FG_OE_5:4
FGROE_7:6 R8 10K FG_OE_7:6
SMB_ADD
CKRPD# R10 10K FG_PD#
FGRSS_EN R11 10K FG_SS_EN

+-- Connect to 1.05V if 1.05 V is available.

VIO3P3
C28 .1uF, C29 .1uF, C30 .1uF, C31 .1uF, C45 .1uF
R35 0
J22 3 Pin Header_0/NS

For VddIO pins.

Vdd3P3 FB1 BLM18AG601SN1D
VFG3P3 C19 10 uF, C20 .1uF, C21 .1uF
R5 1.0
VFG3P3A C22 10uF, C23 .1uF

Do not share ground VIA with other bypass capacitors.
C24 .1uF, C25 .1uF, C26 .1uF, C27 .1uF

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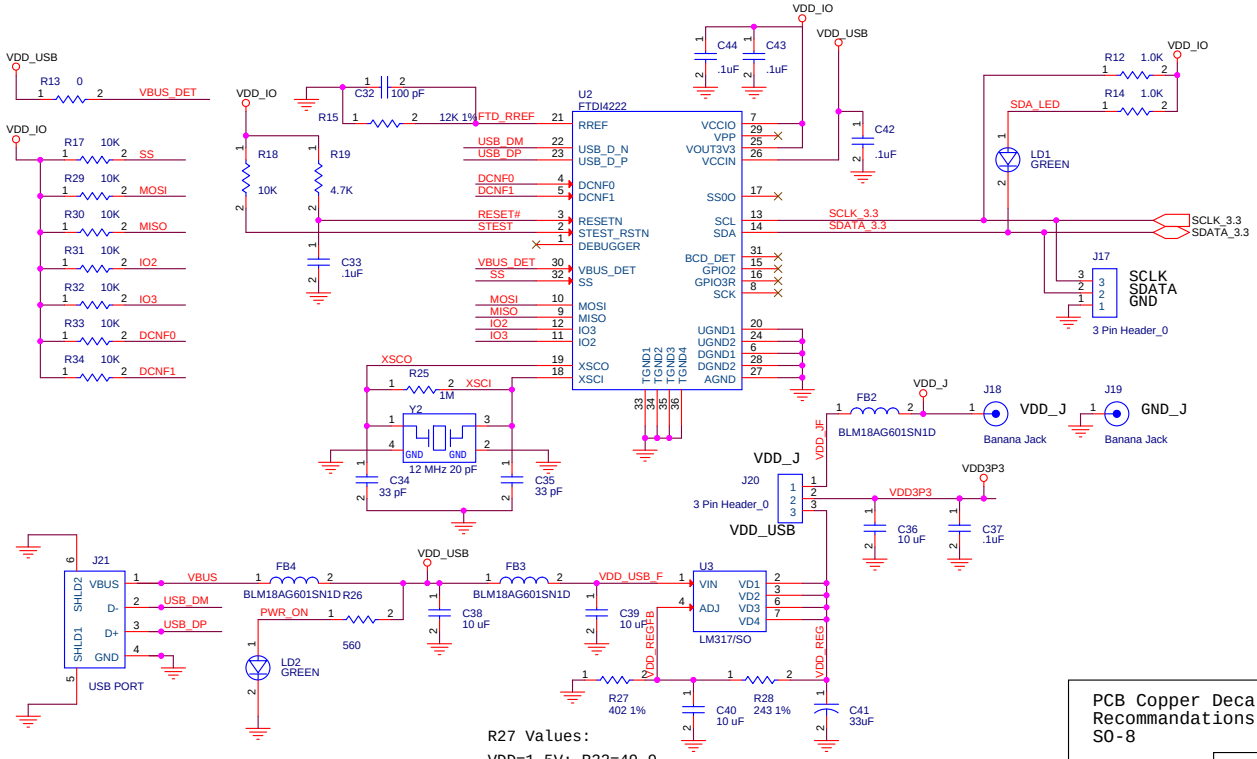
MTH#6_1
NS/MOUNTING HOLE
MTH#6_2
NS/MOUNTING HOLE
MTH#6_3
NS/MOUNTING HOLE
MTH#6_4
NS/MOUNTING HOLE

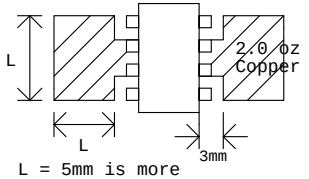
FID1 Fiducial
FIDUCIAL
FID2 Fiducial
FIDUCIAL
FID3 Fiducial
FIDUCIAL



R27 Values:

VDD=1.5V: R22=49.9
VDD=1.8V: R22=107
VDD=2.5V: R22=243
VDD=3.3V: R22=402

PCB Copper Decal Recommandations for LM317LD SO-8



L = 5mm is more than enough

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San Jose, CA

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